Reliability characterization of SiON and MGHK MOSFETs using flicker noise and its correlation with the bias temperature instability

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A B S T R A C T

Bias temperature instability (BTI) is one of the critical device degradation mechanisms in poly-Si/SiON and metal gate/high-k complementary metal-oxide-semiconductor (CMOS) technologies. Using the pre- and post-BTI flicker noise measurements, we investigated the bulk trap density, \( N_t \), in both of these technologies. The low-frequency noise spectra were predominantly of \( 1/f^c \) type with \( c < 1 \) for NMOS and \( /C^24 \) for PMOS. For SiON based technologies, the lower \( V_{TH} \) degradation due to PBTI was noticed while considerable \( V_{TH} \) degradation was observed for NBTI in both SiON and MGHK technologies. Both MGHK and SiON pFETs show a clear increase in the effective volume trap density, \( N_t \), after NBTI. The increase in \( N_t \) in MGHK n-MOSFETs during PBTI is markedly higher than that in MGHK p-MOSFETs during NBTI.

1. Introduction

In downscaled CMOS devices, the use of SiO\(_2\) as a gate dielectric has reached physical limits due to the high leakage currents [1]. The high-\( k \) alternatives for SiO\(_2\) include HfO\(_2\) [2]. However, reliability problems relating to the intrinsic material quality of these dielectrics still exist [1,3–5]. Fluctuations in the channel current are governed by carrier trapping and de-trapping within a few nm from the Si interface [6–7]. As a result, the low-frequency noise has been used as a diagnostic tool for understanding processes and mechanisms affecting device reliability. The low-frequency noise also constitutes a critical technology parameter [8–9]. It can be used to determine the effectiveness of the gate stack when the sources of the current fluctuations are charge trapping – de-trapping events [10–14]. The noise investigations in the past have been focused on the effects of various processing parameters such as the deposition technique, HfO\(_2\) thickness, interfacial layer and type of metal gate on \( 1/f \) noise [15–21]. Various fluctuation processes can be responsible for the \( 1/f \) noise in different materials and devices. For this reason, practical applications of new material systems usually require a thorough investigation of the specific features of the low-frequency noise in the material, and development of methods for its reduction [22–26].

The bias temperature instability (BTI) is one of the important degradation mechanisms in the metal gate high-\( k \) and poly-Si/SiON CMOS technologies and has been studied extensively in the past [27–33]. The bias temperature dependent instability in transistors causes an increase in the threshold voltage of the MOSFET when the device is stressed at higher voltage and high temperature. The threshold voltage shift consequently leads to a decrease in the drain current, which results in the reduced lifetime [34–36]. Flicker noise can be used to investigate newly generated traps as a result of electrical stressing through BTI. In addition, it can be used to investigate dielectric trap distribution and characteristics by utilizing measurements both before and after this stressing.

In this work, we investigate the effect of the BTI stress on \( n \)- and \( p \)-channel MOSFETs with \([i]\) HfO\(_2\) gate oxide and TaN as gate material (MGHK) as well as \([ii]\) SiON dielectric layer with poly-Si gate material (SiON) by using flicker \( (1/f) \) noise measurements. The pre and post BTI effective dielectric volume trap density \( (N_t) \) is also evaluated.

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2. Experimental

The devices used for this study consisted of SiON and metal gate/high-k (MGHK) n- and p-MOSFETs of nominal length with area of 0.06–0.09 $\mu$m². The ratio of the equivalent oxide thickness (EOT) for MGHK to SiON devices was 0.56. The on-wafer noise measurements were carried out in the linear regime at the constant drain voltage $|V_{DS}| = 0.05$ V and the constant drain current values using BTA9812 noise analyzer system in conjunction with NoisePro software from Proplus. Flicker noise on each tested device was measured at three different values of the drain current, $I_D$, corresponding to 10 $\mu$A, 100 $\mu$A and 170 $\mu$A. The charge-pumping measurements were performed on comparable samples by measuring the substrate current while simultaneously applying the voltage pulses of fixed amplitude, rise time, fall time and frequency to the gate.

The BTI stress was applied at a temperature of 125 °C for three different constant voltage stress values: $V_{G1}$, $V_{G2}$, and $V_{G3}$ (where $V_{G3} > V_{G2} > V_{G1}$) applied to n- and p-MOSFET samples. Four devices under test (DUTs) were measured at each voltage condition. The absolute shift in threshold voltage, $\Delta V_{TH}$, was determined at regular intervals, up to the stress time of about 1000 s. All post-stress flicker noise measurements were carried out after a considerable amount of recovery time spanning a number of days.

3. Results and discussion

Fig. 1 shows the normalized $I_D$-$V_G$ characteristics of MGHK and SiON n- and p-MOSFETs. The tested SiON and MGHK n-MOSFETs show a comparable drive current, $I_D$. A similar observation is made for SiON and MGHK p-MOSFETs. Fig. 2 shows the low-frequency (LF) drain current noise spectra ($S_{ID}$) comparison of MGHK and SiON n-MOSFETs while Fig. 3 presents the comparison for MGHK and SiON p-MOSFETs. The data are the average values of the current spectral density, $S_{ID}$, for multiple samples measured at three different drain currents $I_D$. Fitting is carried out at the $V_G \sim V_{TH}$ condition, which corresponds to the drain current $I_D = 10$ $\mu$A. For SiON and MGHK MOSFETs, the LF noise spectra follow $1/f^\gamma$ type dependence, where p-MOSFETs have $\gamma \sim 1.04$–1.09. It has been established in prior studies that when $\gamma \sim 1$, the traps are evenly distributed through the tunneling distance and the energy band gap [37,38]. The tested SiON and MGHK n-MOSFETs reveal $\gamma \sim 0.83$, which suggests that there is a larger number of higher frequency traps, and the distribution of these traps is skewed closer to the dielectric interface [37,38]. Fig. 4 shows the average low-frequency noise values for multiple samples at $f = 25$ versus the drain current ($I_D$) that they were measured at. This allows us to see the transition from weak to moderate/strong inversion. Noise levels were seen to be similar for SiON and MGHK n-MOSFETs at every drain current $I_D$. The same can be seen for SiON and MGHK p-MOSFETs.

Assuming a trapping origin of 1/f noise, the effective volume trap density, $N_t$, can be estimated from the input-referred noise spectral density, $S_{NVF}$, using the formula

$$S_{NVF} = \frac{q^2 k T N_t}{W L C_{inv}^2 \chi f^\gamma},$$

where $k$ is the Boltzmann constant, $T$ is the absolute temperature, $q$ is the electron charge, $C_{inv}$ is the inversion capacitance per unit area given by $C_{inv} = \varepsilon_{ox} \varepsilon_0 A_{inv}$, $\varepsilon_{ox}$ is the permittivity of SiO₂, $\chi$ is the tun-
The surface trap density, $D_t$, was estimated as

$$D_t = 4kTzN_t,$$

where $z$ is the tunneling distance of the carrier from the Si/high-k interface. It is evaluated at $f = 25$ Hz to be $1.49$ nm for SiON and $2.08$ nm for MGHK MOSFETs, respectively and was calculated using the formula

$$\frac{1}{2I_f} = \tau_a \exp(\alpha z).$$

The value of the tunneling parameter $\alpha$ was $1.2 \times 10^{6}$ cm$^{-1}$ and $0.86 \times 10^{6}$ cm$^{-1}$ for SiON and MGHK MOSFETs, respectively. The calculated noise parameters are shown in Table 1 while the final calculated values of $N_t$ and $D_t$ are indicated in Table 3. The charge pumping measurements were performed on comparable samples to estimate the interface state density, $N_{is}$, using the formula

$$N_{is} = \frac{I_{cp}}{qA},$$

where $I_{cp}$ is the charge pumping current, $f$ is the test frequency, and $A$ is the channel area (in cm$^2$ units) [41]. The calculated interface state density, $N_{is}$, was found to be comparable to the previously calculated pre-stress surface trap density values, $D_t$, that were extracted from the flicker noise measurements, as shown in Table 3.

**Fig. 5.** $\Delta V_{TH}$ versus stress time at $125^\circ C$ for various stress voltages showing $V_{TH}$ degradation in MGHK n- and p-MOSFETs. There is a clear correlation between applied stress and $\Delta V_{TH}$ for both PBTI and NBTI.

Table 1

<p>| Noise parameters: values at $V_{GS} \sim V_{TH}, |V_{DS}| = 0.05$ V, Freq = 25 Hz. |
|--------------------------------------------------|</p>
<table>
<thead>
<tr>
<th>$S_{vis}$ (V$^2$/Hz)</th>
<th>$Z$ (nm)</th>
<th>$\alpha_t$ (1/cm)</th>
<th>$C_{inv}$ (F/cm$^2$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>N-MGHK</td>
<td>$1.39 \times 10^{-10}$</td>
<td>2.08</td>
<td>$0.86 \times 10^{-3}$</td>
</tr>
<tr>
<td>P-MGHK</td>
<td>$1.18 \times 10^{-10}$</td>
<td>2.08</td>
<td>$0.86 \times 10^{-3}$</td>
</tr>
<tr>
<td>N-SiON</td>
<td>$9.99 \times 10^{-11}$</td>
<td>1.49</td>
<td>$1.2 \times 10^{3}$</td>
</tr>
<tr>
<td>P-SiON</td>
<td>$2.38 \times 10^{-10}$</td>
<td>1.49</td>
<td>$1.2 \times 10^{3}$</td>
</tr>
</tbody>
</table>

show considerable $\Delta V_{TH}$ shift for MGHK n- and p-MOSFETs. It can be seen that PBTI $\Delta V_{TH}$ is much higher at each applied stress value, and it peaks at $\sim 100$ mV at the applied stress voltage of $V_{G3}$. The NBTI $\Delta V_{TH}$ peaks at $\sim 65$ mV at the same applied stress voltage.

**Fig. 6.** The absolute threshold voltage shift for SiON n- and p-MOSFETs at $125^\circ C$ under different stress conditions and different time intervals. Unlike the MGHK type devices where both n- and p-type devices show clear threshold voltage shift, only SiON p-MOSFETs under NBTI were observed to have significant $\Delta V_{TH}$ at three different applied stress conditions, reaching a peak of $\sim 32$ mV at stress time $\sim 1000$ s and under an applied stress corresponding to $V_{G3}$. PBTI reveals lower $\Delta V_{TH}$ degradation.

The flicker noise measurements for post-BTI devices can be used to investigate newly generated traps [42]. Fig. 7 and Fig. 8 present the pre- and post-BTI low-frequency noise spectra for n- and p-type MGHK and SiON MOSFETs for a given voltage $V_{G3}$ after 1000 s stress respectively. In all cases, a slight increase in the newly generated traps is observed post-stress except for the SiON p-MOSFET where a larger increase observed, leading to the increased drain current noise spectral density after the stress. The effective volume trap density post-BTI at $25$ Hz for devices stressed to $V_{G3}$ is calculated following the method described earlier. It is compared to the $N_t$ value determined pre-BTI. The pre- and post-stress results are shown in Table 3.

**Table 3**

<table>
<thead>
<tr>
<th>Stress time [s]</th>
<th>$\Delta V_{TH}$ [mV]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1000 s</td>
<td>32 mV</td>
</tr>
<tr>
<td>10000 s</td>
<td>65 mV</td>
</tr>
</tbody>
</table>

From Table 3, one can see that the MGHK PBTI reveal a larger increase in $N_t$ than NBTI. The data indicate that MGHK n- and p-MOSFETs have the increased density of interface traps as a result of the electrical stressing. The latter explains the appearance of the generation-recombination humps in the post-BTI spectra as the capture and emission of carriers through these newly generated traps causes fluctuations in the number of free carriers. The trapped charge can also cause fluctuations in the mobility, electric field and barrier height.

A comparison of the extracted $N_t$ post-BTI in SiON MOSFETs (Table 3), calculated at $f = 25$ Hz, indicate that NBTI creates higher density of interface traps compared to PBTI. The shift $\Delta V_{TH}$ for NBTI in SiON MOSFETs is comparable to conventional MGHK devices. However, SiON devices under PBTI show the lower threshold voltage shifts, close to the operation condition. The exception is the high-voltage stress, close to the dielectric breakdown, at which point the instability can be observed at shorter stress times [34].

**Fig. 4.** Drain current noise versus drain current characteristics for MGHK and SiON n- and p-MOSFETs.
This effect can be attributed to the bulk defect generation in the gate oxide.

The absolute threshold voltage $\Delta V_{TH}$ of the MOSFET increases while the device is biased in the inversion mode [34]. There are distinct differences in the physical degradation mechanisms between PBTI and NBTI due to the defect structure of the dielectric, asymmetry in the band structures of the Si/high-$k$/metal gate stack and the opposite polarity of the gate bias [34]. During NBTI in p-MOSFETs, hole trapping and interface state generation have been observed [36] with the physical degradation process involving hole trapping in the dielectric layer and interface-state generation at the interface for both MGHK and SiON MOSFETs. The basic degradation mechanism for both MGHK and SiON MOSFETs is similar. The positive charges can be trapped at interface and near-interface states (border traps), as well as in the bulk of the oxide. The trapped charges, which are very close to the inversion layer, lead to degradation in the channel carrier mobility due to Coulomb scattering effect. As a result of the mobility degradation, the peak transconductance of both MGHK and SiON devices in the linear regime decrease with increasing voltage shift. This would explain why both MGHK and SiON p-MOSFETs show an increase in effective dielectric volume trap density $N_t$ after NBTI.

On the other hand, during PBTI on n-MOSFETs, MGHK devices show electron trapping in the high-$k$ layer and/or the region between the high-$k$ layer and the interfacial oxide layer [43] while electron trapping is seen to be small or negligible in SiON devices. For this reason, we see an increase in $N_t$ in MGHK n-MOSFETs during PBTI that is markedly higher than the increase of $N_t$ in SiON n-MOSFETs. The degradation features vary for NBTI and PBTI due to difference in the charge location [36]. The Coulomb scattering is generally weaker since trapped charge is separated from the inversion channel by the interfacial oxide layer [36]. This means that the channel carrier mobility remains constant, independent of the amount of trapped charge. For this reason, the transistor characteristic is only horizontally shifted on the voltage scale.

### Table 2

<table>
<thead>
<tr>
<th>Applied $V_C$ (V)</th>
<th>N-MOSFET</th>
<th>P-MOSFET</th>
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<tbody>
<tr>
<td>$V_{G1}$</td>
<td>~10</td>
<td>~8</td>
</tr>
<tr>
<td>$V_{G2}$</td>
<td>~40</td>
<td>~30</td>
</tr>
<tr>
<td>$V_{G3}$</td>
<td>~100</td>
<td>~65</td>
</tr>
</tbody>
</table>

### Table 3

<table>
<thead>
<tr>
<th>Stress time [s]</th>
<th>Pre-stress</th>
<th>Post-stress</th>
</tr>
</thead>
<tbody>
<tr>
<td>$N_t$ (1/cm³)</td>
<td>1.34 × 10¹⁸</td>
<td>1.80 × 10¹⁸</td>
</tr>
<tr>
<td>$D_t$ (1/cm²)</td>
<td>2.93 × 10¹⁰</td>
<td>3.93 × 10¹⁰</td>
</tr>
</tbody>
</table>

Fig. 6. $\Delta V_{TH}$ versus stress time at 125 °C for various stress voltages showing $V_{TH}$ degradation on SiON n- and p-MOSFETs. PBTI for these devices is not seen to cause any clear or significant $\Delta V_{TH}$. There is a clear correlation between applied stress and $\Delta V_{TH}$ for NBTI.

Fig. 7. Pre- and Post-BTI low-frequency noise spectra at $|V_{DS}| = 0.05$ V for n- and p-MGHK MOSFETs. Post-stress values shown are for $V_{G3}$ after 1000 s. Note the enhanced $S_{D0}$ change during BTI in p-MOSFETs as opposed to n-MOSFETs.

Fig. 8. Pre- and Post-BTI low-frequency noise spectra at $|V_{DS}| = 0.05$ V for n- and p-MGHK MOSFETs. Post-stress values shown are for $V_{G3}$ after 1000 s. Note the enhanced $S_{D0}$ change during BTI in p-MOSFETs as opposed to n-MOSFETs.
4. Conclusions

In this work, the flicker noise measurements were used as the diagnostic tool for understanding MGHK and SION MOSFETs in terms of the correlation between bulk trapping density (Nt) and BTI. The increase in Nt was seen in all cases after electrical stressing with a larger increase seen with PBTI as compared to NBTI in MGHK devices. A symmetric trap distribution was observed for MGHK and SION p-MOSFETs while the tested n-MOSFETs exhibited an asymmetric trap distribution. An analysis of the threshold voltage shift $\Delta V_{TH}$ of the different types of MOSFETs under BTI was performed. Both n- and p-type devices show clear threshold voltage shift under BTI while only SION p-MOSFETs under NBTI were observed to have significant threshold voltage shift at applied stress conditions. Finally, a comparison between the physical degradation mechanisms in these MOSFETs was used to explain calculated values of Nt.

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References

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