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Variability Effects in Graphene: Challenges and Opportunities for Device Engineering and Applications

The authors address the origin of variabilities in graphene devices and how these variabilities contribute to device performance fluctuations and noise.

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ABSTRACT | Variability effects in graphene can result from the surrounding environment and the graphene material itself, which form a critical issue in examining the feasibility of graphene devices for large-scale production. From the reliability and yield perspective, these variabilities cause fluctuations in the device performance, which should be minimized via device engineering. From the metrology perspective, however, the variability effects can function as novel probing mechanisms, in which the ''signal fluctuations'' can be useful for potential sensing applications. This paper presents an overview of the variability effects in graphene, with emphasis on their challenges and opportunities for device engineering and applications. The discussion can extend to other thin-film, nanowire, and nanotube devices with similar variability issues, forming general interest in evaluating the promise of emerging technologies.

KEYWORDS | Device engineering; device scalability; edge disorder; graphene; interface traps; low-frequency noise; metrology; sensing applications; variability effects

I. INTRODUCTION

Graphene draws considerable interest in electronics, photonics, and multiple cross-fields owing to its combination of exceptional properties [1]: high carrier mobility [2], [3], atomically thin planar structure [4], linear dispersion of Dirac fermions [5], high mechanical strength [6], high thermal conductivity [7], and potential low cost [8]–[10], among others [11]. Raised by the rapid progress of material synthesis and fabrication techniques [9], [12]–[15], graphene has shown its potential in wafer-scale radio-frequency analog circuits [16]–[23], broadband photodetection [24]–[26], electronic circuit interconnects [27]–[29], thermal management [30]–[33], and sub-nanometre trans-electrode membrane for DNA detection [34]–[36]. To date, graphene-based materials, generally referred to graphene, graphene nanoribbon, graphene oxide, and some others [1], are the focus of nanoscience and nanotechnology societies, with continuous efforts on exploring their versatile applications [1], [11], [37]–[40].

Manuscript received May 3, 2012; revised December 1, 2012 and February 6, 2013; accepted February 13, 2013. Date of publication March 26, 2013; date of current version June 14, 2013. This work was supported in part by the SRC-DARPA MARCO Focus Center on Functional Engineered Nano Architectonics (FENA) and the U.S. Department of Energy under Contract DE-AC02-05CH11231.

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Digital Object Identifier: 10.1109/JPROC.2013.2247971

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Increasing process variability poses a major challenge to the continued scaling of semiconductor technology (e.g., limits the reliability and yield); addressing this issue requires optimization of both device and circuit designs [41]–[47]. Variability sources in the standard complementary metal–oxide–semiconductor (CMOS) process can be categorized according to their spatial characteristics, time scales, physical/environmental origins, and systematic/random components [42], [43], [46]. In addition, the nature of variability is likely to change with the progress of innovative materials, fabrication methods, and device structures in the targeted applications [46], [48]–[52]: some variability sources may diminish while others may emerge; some can be minimized via device engineering (e.g., variation in nominal lengths/widths), while others are limited by the material imperfection (e.g., interface roughness and dopant fluctuation). The identification, characterization, and evaluation of variability effects in emerging technologies are essential in examining their ultimate promises for large-scale production [53]–[56].

Motivated by the potential of graphene as a material candidate to incorporate into silicon devices for high-speed electronics and integrated photonics [40], there has been considerable interest on the variability effects in graphene and graphene-related technology [12], [51], [57]–[60]. At the moment, efforts are made on the characterization of graphene variabilities in the prototyped device structures and the evaluation of their effects on the device performance [60]–[65]. However, a systematic discussion of the variability sources in graphene and their impact on circuits and systems are rare. From the reliability perspective, these variabilities in graphene cause device fluctuations and are detrimental to the yield in large-scale production. It is, therefore, crucial to seek ways of minimizing their effects via device engineering (e.g., adjusting the process flow or device structure), one topic that is being heavily investigated [12], [60], [63], [64], [66]–[70]. From the metrology perspective, on the other hand, we demonstrate that variabilities in graphene can function as novel probing mechanisms [58], [65], [71]–[75], where the "signal fluctuations" can be useful for potential sensing applications. This role of graphene variabilities is of both fundamental and practical interest [76]–[78], extendable to other thin films or nanomaterials [79]–[82], and may be employed in developing novel metrology applications.

With this introduction, here we review the status and prospects of variability effects in graphene, discussing their challenges and opportunities for device engineering and applications, respectively. Section II provides an overview of variability sources in graphene, with emphasis on their concepts, categorizations, and the comparison with those in silicon devices. Two broad classes of variabilities in graphene, those from the environmental disturbance and those from the material imperfection, are described with typical examples. For the first class, Section III reviews the variabilities originating from the interface traps close to the graphene surface. These variabilities broadly exist in nonsuspended graphene devices, and are of particular significance to evaluate the device stability. We discuss their physical principles, characterization methods, and the approach to minimize their effects via device engineering. For the second class, Section IV reviews the variabilities originating from the edge disorders within graphene itself, which represent the variation sources limited by material preparations. We examine the concepts of edge disorders, their effects on device performance, and ways of reducing them by improving the material quality. Section V reviews graphene variabilities from the metrology perspective. We present the possible use of the "signal fluctuations" as novel probing mechanisms for sensing applications (e.g., probing the band structure, selective chemical sensing), and outlook their potential in nanometrology. Section VI concludes the paper with several further discussions.

II. VARIABILITY SOURCES IN GRAPHENE

Graphene variabilities can be fundamentally viewed as sources/mechanisms that lead to deviations of the functional behavior from its ideal case [5]. We note that graphene can bear fluctuation mechanisms such as thermal noise, shot noise, and electron–phonon/electron scatterings [83]–[86], which belong to the inherent properties of graphene and are out of the scope of our discussions.

Variability sources due to the nonideality of graphene can be categorized into two broad classes (see Table 1).

I) Variabilities from the environmental disturbance are located close to the graphene surface and

Table 1 Typical Variabilities in Graphene. Variability Sources Due to the Nonideality of Graphene Can Be Categorized Into Two Broad Classes: Those From the Environmental Disturbance and Those From the Imperfection of Material Quality

Typical Variabilities in Graphene
I) Variabilities from the environmental disturbance:
1) Interface traps [65]
2) Charged impurities [87, 88]
3) Adsorbed molecules [89]
4) Resonant scatterers [90]
5) Surface roughness [3]
6) Contact doping [64]
II) Variabilities from the material imperfection:
1) Edge disorders [91]
2) Structural defects away from the edge [92]
3) Ripples [93]
4) Curvatures [94]
5) Other derivatives of graphene [95]

significantly affect the device properties (e.g., mobility, doping) [3], [64], [65], [87]–[90]. These variabilities are attributed to the external perturbations of the environment surrounding the graphene channel, such as the dielectric layer, the ambient environment, and the substrate.

II) Variabilities from the imperfection of material quality are randomly distributed in graphene itself [91]–[95]. These variabilities are attributed to the geometrical variations of the graphene material, posed by the limit of synthesis and preparation methods.

It is instructive to compare the aforementioned variability sources in graphene with those in silicon technology [42], [43], [46], [96]–[99]. Both class I and II graphene variabilities are analogous to the random variations in silicon devices (i.e., device parameter fluctuations in an unpredictable manner), however several differences exist between the sources of graphene and silicon variabilities. For example, some of class I graphene variabilities (e.g., adsorbed molecules, surface roughness) are less problematic in silicon devices [43]. The variabilities near the graphene-dielectric/substrate interface have attracted considerable interest in graphene communities, mostly because they are: 1) more influential in low-dimensional graphene devices with high surface-to-volume ratios [62], [71], and 2) relatively less understood than the $Si–SiO_2$ interface in CMOS technology [52]. Moreover, class II graphene variabilities are the randomness specific to the handling of graphene materials, which are not exactly the same as those in silicon devices [43], [55], [100], [101]. For instance, edge disorders in graphene are not normally addressed in silicon devices possibly due to the maturity of CMOS technology. And the graphene-on-insulator or suspended graphene device structures are relatively immune from the random dopant fluctuation in the bulk silicon, one major random variation in CMOS processes. The differences between graphene and silicon variabilities need to be taken into account when integrating these two materials [40]. On the other hand, current research on graphene variabilities has focused on the device level up to the within-die and die-to-die scales [51], [57], whereas studies on the circuit and system levels in the wafer-to-wafer scale are still rare. Many systematic variations in silicon technology (i.e., definite spatial or temporal shifts caused by the tolerance of fabrication processes) would also be critical in the device engineering of graphene, such as length/width variations in lithography and etching steps, film thickness variations in deposition, and growth processes, among others [42], [46], [99]. The related works would be crucial in evaluating the promise of graphene electronics.

Our discussions provide an overview of the similarities and differences between the variabilities in graphene and those in silicon. The nature of variability effects in graphene lies in its low dimension and ways of preparing the material. The field is new, rapidly growing, and full of ample research opportunities. In the following, we will present the progress of two graphene variabilities, interface traps (class I) and edge disorders (class II), which have shown their critical roles in achieving high-performance graphene devices (Sections III and IV) and opportunities for potential sensing applications (Section V).

III. INTERFACE TRAP: GRAPHENE VARIABILITIES FROM ENVIRONMENTAL DISTURBANCE

Due to their large surface-to-volume ratio, graphene devices are sensitive to the interface traps close to the graphene surface [61], [71], [77]. They exist in the gate oxide or the substrate of nonsuspended graphene devices, and can also be from the attached molecules or the surrounding environment [60]–[62], [70], [102]. Similar to silicon technology, trap-induced fluctuations in graphene pose a challenge to the device scalability since their effect increases as the device scales down [42], [103]. We next discuss their principles, characterization methods, and how to minimize their effects via device engineering.

A. Device Fluctuations Caused by a Single Interface Trap

If a single trap close to the channel has its energy near the Fermi level ($\sim k_B T$, here k_B is Boltzmann's constant and T is the absolute temperature), the device signal (e.g., current) will show two-level fluctuations in the time domain [see Fig. 1(a)] [103]–[106]. The random switching events (i.e., capture and emission of a single carrier from the channel by the trap) follow the Poisson statistics. In the frequency domain, the power spectrum density (PSD) has a form of $S(f) = g \cdot \tau / (1 + (2\pi f \tau)^2)$ with a corner frequency and a prefactor as $f_{\text{corner}} = 2\pi\tau = 2\pi(\tau_1^{-1} + \tau_2^{-1})^{-1}$ and $g = (4\tau_1\tau_2/(\tau_1+\tau_2)^2) \cdot (\Delta i)^2$ (Δi is the current step in the time domain; $\tau_{1,2}$ are the time constants of the two states), respectively [104], [106]. This Lorentzian-shape PSD is nearly constant when $f \ll f_{\text{corner}}$, and approximately follows as $1/f^2$ when $f \gg f_{\text{corner}}$ [see Fig. 1(b)].

These two-level fluctuations belong to random telegraph noise (i.e., RTN, generation/recombination noise) [107]–[109]. It is commonly measured by sampling the current variations in the time domain under a constant voltage bias across the channel (i.e., source-drain voltage) [105], [107]. RTN is a critical issue to the signal-to-noise ratio of devices due to its increasing effect with device scaling. However, RTN in graphene has not been systematically investigated at this stage, whereas many studies have been reported in carbon nanotube (CNT) [110]–[112]. The reason may be that the enclosed structure of CNT with a small diameter (2–5 nm) can have fewer interface traps than a planar graphene sheet with a micron-sized width. RTN might be observable in small-area graphene devices at low temperature, such as a graphene nanoribbon with a nanometer-sized width [13], [14].

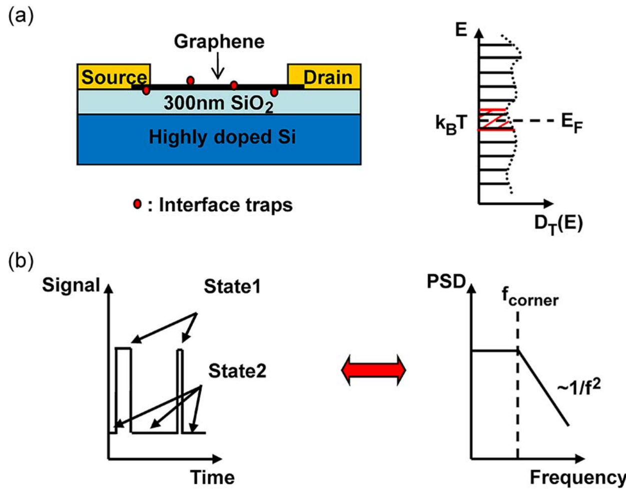

Fig. 1. ***Device fluctuations caused by a single interface trap. (a) Left panel: Schematics of a back-gated graphene device fabricated on a SiO_2/Si substrate. The interface traps (red dots) are located close to the graphene surface. Right panel: Schematics of the density of trap states (D_T) in the energy scale (E). The traps with energy near the Fermi level ($\sim k_BT$) can cause the random switching events, which lead to device fluctuations. (b) Left panel: Two-level signal fluctuations in the time domain caused by a single interface trap (RTN). The time constants of the two states are labeled as $\tau_{1/2}$. Right panel: A typical Lorentzian-shape PSD of RTN in the frequency domain. The PSD exhibits a corner frequency (f_{corner}) and a near $1/f^2$ shape beyond f_{corner}.***

B. Device Fluctuations From Many Interface Traps

Multiple-level fluctuations, on the other hand, are usually characterized by low-frequency noise measurement (LFN) in the frequency domain (typically from 0.1 to 100 kHz) [113]–[115]. Although other physical mechanisms of LFN may coexist [109], [116], [117], interface traps are usually employed to understand the origin of LFN in graphene devices [61], [65], [102], [118], [119]. For instance, suspended graphene devices show a 6–12 times lower LFN than those with a SiO_2 substrate, suggesting that the traps in SiO_2 substrate contribute significantly to LFN [118]. On the other hand, recent studies have suggested that the LFN in graphene depends on various scattering mechanisms, the environment near the graphene surface, and the sample qualities [65], [77], [102], [119]. For instance, Heller *et al.* [102] have proposed that the LFN behavior in liquid-gated graphene devices can relate to the charge-induced local potential fluctuations near the graphene–electrolyte interface (i.e., the charge noise).

The McWhorter model views the LFN as the multilevel fluctuations caused by an ensemble of many interface traps (number $\gg 1$): each trap contributes an RTN over a wide range of τ and f_{corner} [see Fig. 2(a)] [109], [117], [120], [121]. The overall PSD can be integrated as $S(f) = \int_\tau g \cdot \tau/(1+(2\pi f\tau)^2) \cdot p(\tau) d\tau$, where $p(\tau)$ is the distribution function of τ. Assuming that 1) electrons reach the traps by tunneling and τ depends exponentially on the distance from the channel (z), one has $\tau = \tau_0 \exp(z/\lambda)$ (λ is the penetration depth), and 2) traps are uniformly distributed along the z-direction (i.e., $dN_T/dz = \text{const.}$ with N_T as the number of traps) [113], [117], one has $p(\tau) \sim (dN_T/d\tau) = (dN_T/dz) \cdot (dz/d\tau) = (dN_T/dz) \cdot (\lambda/\tau)$ and $S(f) \propto \int_\tau 1/(1+(2\pi f\tau)^2) d\tau \propto (1/f)$, which is known as the $1/f$ noise. The McWhorter model is physically intuitive and popular in LFN theorem, but it only holds when LFN is dominated by the carrier number fluctuations [113], [117], [121]. At present, it is still unclear about the relative contribution of carrier number fluctuations to the overall LFN in graphene devices.

The importance of LFN for practical applications stems from the fact that it contributes to the phase noise of the devices and systems via unavoidable nonlinearity. A low-level phase noise is a critical requirement for high-frequency applications of graphene [61], [122]. LFN measurements are broadly used as a characterization technique to provide information about interface traps in graphene devices [60], [61], [63], [65], [77], [123]. Fig. 2(b) and (c) shows a typical room-temperature LFN measurement of a back-gated single-layer graphene (SLG) device [65]. The study employed a four-probe configuration to minimize the noise contribution from the contacts (see the inset of Fig. 2): an Agilent 4156C was used to apply dc current bias to the device, and measure its dc conductivity σ; an Agilent 35670A was used to collect the noise spectra of the fluctuations of the potential difference (V) across the graphene samples. At each gate bias (shifted by V_{Dirac}, the gate bias at Dirac point), the conductivity was averaged ten times at the same time of the noise measurement in order to ensure the data consistency [see Fig. 2(b)]. The noise spectra (S_V) were averaged 20 times from the fast Fourier transforms of the sampled voltage signal (V), and subtracted by the background measured at zero current bias [see Fig. 2(c)]. The measured LFN followed the $1/f$ shape (i.e., $1/f^\alpha$, $\alpha \sim 1$) at each gate bias, whereas the deviation may relate to pronounced Lorentzian spectra from individual RTNs or other noise sources.

To quantify the data, we can normalize LFN as $(S_I/I^2)_{V=\text{const.}} = S_G/G^2 = S_R/R^2 = (S_V/V^2)_{I=\text{const.}} = A/f^\alpha$ by assuming the resistance/conductance (R/G) is independent from the bias condition [109]. Parameter A is commonly used as a measure of the LFN amplitude [61], [65], [115], [124]. Alternatively, Hooge parameter α_H is empirically defined as $(S_I/I^2)_{V=\text{const.}} = A/f^\alpha = \alpha_H/(f^\alpha N)$ (N is the total number of carriers), whose value depends on the details of the materials and devices [116], [125], [126]. As such, Table 2 summarizes the typical LFN measurements in graphene and graphene nanoribbon (GNR) devices [61], [63], [65], [70], [77], [123]. The measured α_H value (from 10^{-5} to 10^{-2}) depends on many factors such as contact material, device environment, and sample quality. For example, the noise in chemical vapor deposition (CVD)-based graphene devices ($\alpha_H \sim 8-9 \times 10^{-3}$) can be comparable to that in exfoliation-based graphene

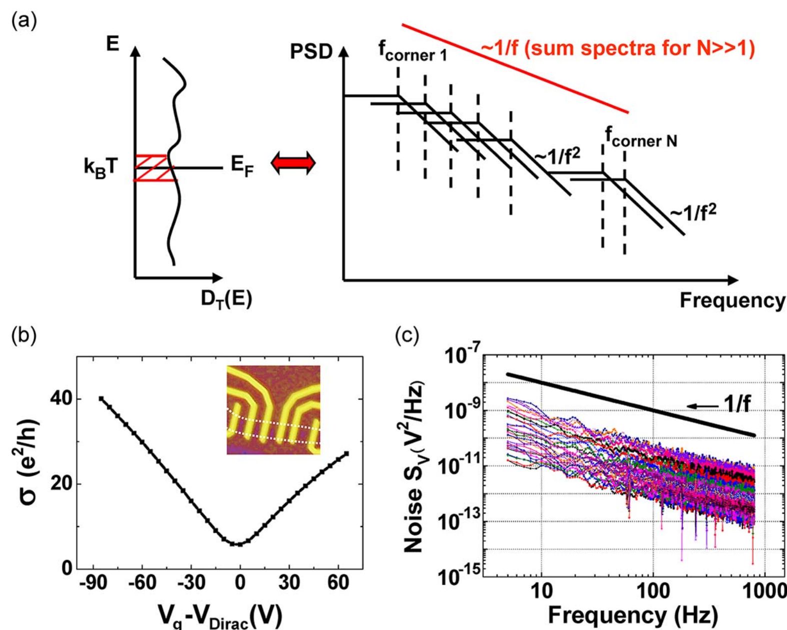

Fig. 2. ***Device fluctuations from many interface traps. (a) Schematics of the McWhorter model. Left panel: If there are many interface traps with energy close to Fermi level (several k_BT), all of them will contribute to the carrier trapping/detrapping processes. Right panel: An ensemble of many trap-induced RTNs with a wide range of time constant and corner frequency ($f_{\rm corner}$) can result in LFN with a $1/f$ shape of PSD. (b) The dependence of direct current (dc) conductivity (σ) on the gate bias (V_g) measured in an SLG device under four-probe configuration (shifted by the gate bias at the Dirac point $V_{\rm Dirac}$) [65]. The inset shows the optical image of a fabricated multiterminal device (graphene was outlined in dotted lines). (c) Typical room-temperature LFN spectra of a back-gated graphene sample [65]. The four-probe noise spectra (S_V) followed $1/f^\alpha$ behavior with α ranging from 0.85 to 1.12 with gate biases varying from -50 to 100 V.***

devices ($\alpha_H \sim 10^{-3} - 10^{-2}$) [65], [70], [77]. This result suggests a low amount of impurities left on graphene during the CVD growth and transfer processes (much better than previous results [127]). On the other hand, bilayer GNRs (BLR) were reported to exhibit a lower noise than SLRs, which can relate to their different band structures and transport properties [61], [128].

C. Approach to Minimize the Effect of Interface Traps

Trap-induced fluctuations in graphene degrade the device performance, forming a critical issue that needs to be addressed. Many efforts are made to minimize their effect via device engineering, which include device passivation [63], the use of multilayer graphene (MLG)

Table 2 Typical α_H Values in Graphene and GNR Devices at Room Temperature. The Measured α_H Value (From 10^{-5} to 10^{-1}) Depends on Factors Such as Contact Material, Device Environment, and Sample Quality. The LFN Data Were Measured in Either Dual-Gated [63] or Back-Gated Devices [61], [65], [70], [77], [123]. Abbreviations: Single-Layer Graphene (SLG); Bi-Layer Graphene (BLG); Few-Layer Graphene (FLG); Multi-Layer Graphene (MLG); Single-Layer GNR (SLR); Four-Probe Measurement (4T)

Data source	Contact	$L_{channel}$ (μm)	Exposure	Sample	Typical Mobilities (cm^2/(Vs))	α_H (away from Dirac point)
G. Liu [63]	Cr/Au (2T)	9	Ambiance + HfO_2 TG	SLG	μ_e~1550 μ_h~2200	2×10^{-3}
Q. Shao [123]	Cr/Au (2T)	9	Ambiance	BLG	$\mu_{e/h}$~3000	~1×10^{-4}
A. N. Pal [70]	Au (4T)	~2-4 (Fig. 1b)	Vacuum	SLG/ FLG/MLG	~1100 (SLG), ~2450(FLG), ~1200(MLG)	2×10^{-2}(SLG), 5-8$\times10^{-5}$(FLG /MLG)
Y. M. Lin [61]	Pd (2T)	0.8-2.8	Vacuum	SLR/BLR	~700 (SLR)	~10^{-3}(SLR)
G. Xu [65]	Ti/Au (4T)	1.5-2.8(SLG) 1.9-5.5(BLG)	Vacuum	SLG/BLG	~2000-4000(SLG) ~1000-5000(BLG)	~10^{-3}-10^{-2} (SLG/BLG)
A. N. Pal [77]	Au (4T and 2T)	15	Vacuum	CVD-based SLG	~400 at room temperature	8~9$\times10^{-3}$

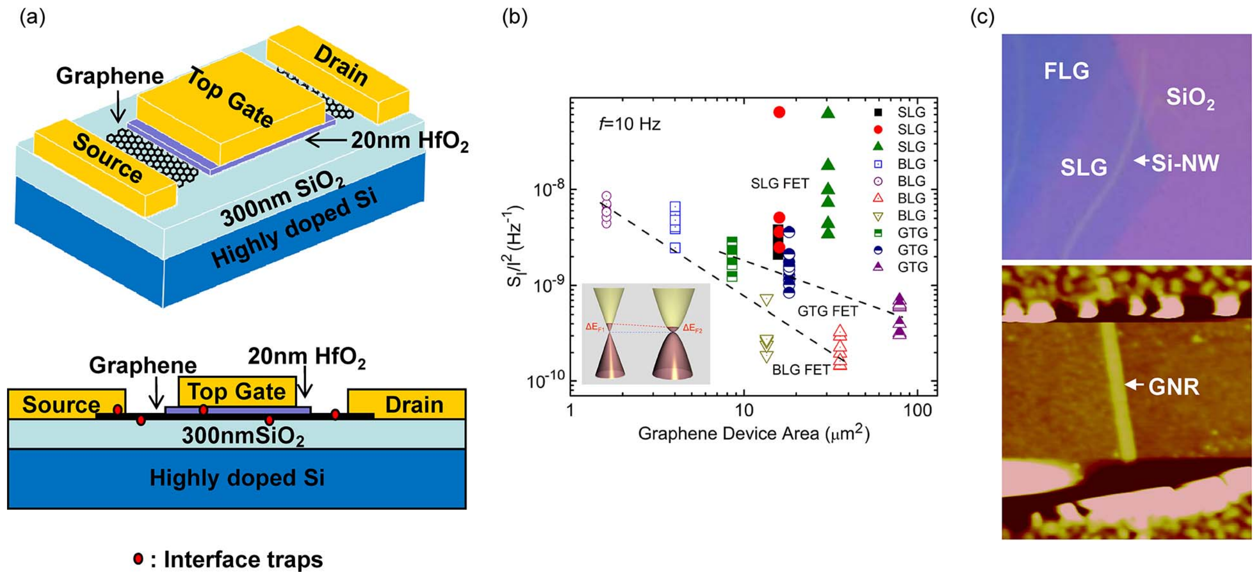

Fig. 3. *Device engineering to minimize the effect of interface traps in graphene devices. (a) Top panel: A dual-gated SLG device with a SiO_2/Si substrate (back gate) and a 20-nm HfO_2 layer as the top-gate dielectric [63]. Bottom panel: The low-noise SLG devices ($\alpha_H \sim 10^{-3}$) benefit from the top-gate passivation, where the noise was mainly from the ungated graphene channel. (b) Comparison of the normalized LFN values (S_I/I^2 at $f = 10$ Hz with $|V_g - V_{\text{Dirac}}| \leq 30$ V) in GTG, SLG, and BLG devices [64]. The lower noise in GTG (than that in SLG) can be from the reduced noise contribution near the contact with more layers. (c) Top panel: The optical image of the silicon nanowires patterned onto single layer (light blue) and multilayer (dark blue) bulk graphene sheet on top of 300-nm SiO_2 layer (purple) [60]. Bottom panel: The AFM image of a typical BLR after removal of the nanowire mask (Ti/Au contacts). This fabrication method avoided the photoresist contamination (e.g., HSQ) to the GNR surface, which helps lower the noise.*

channels [64], [70], surface cleaning [60], and substrate engineering [3], [118].

A recent study has reported the measurements of LFN in the double-gated graphene devices, which helped to understand the effect of passivation on the noise level [63] [see Fig. 3(a)]. SLG sheets (width ~ 10 μm) were exfoliated from highly oriented pyrolytic graphite onto a thermally grown 300-nm SiO_2 dielectric layer on a highly doped Si substrate which acts as the backside gate (BG). A 20-nm HfO_2 layer achieved by atom-layer deposition (ALD) method was used as the top-gate dielectric, which was patterned by electron-beam lithography to partially cover the graphene channel. The Cr/Au metal layers (5/60 nm) were evaporated to serve as the source, drain, and top-gate electrodes. A two-terminal LFN measurement was conducted in ambience by monitoring the PSD of the current (S_I) with a constant drain-to-source bias (V_{ds}). The devices benefit from the top-gate passivation by the HfO_2 layer, where the gated channel is immune to the possible traps from ambiance. The measured LFN was low ($\alpha_H \sim 10^{-3}$), and found to be mainly due to the ungated graphene channel (i.e., uncovered by the HfO_2 layer). This result suggests that a low-noise graphene device can be achieved by improving the passivation of the channel.

Using MLG (i.e., > 1 layer) as the channel material is another approach to achieve low-noise devices. For example, a graphene sheet with more than three layers [few-layer graphine (FLG)] has been found to have much lower LFN than that in SLG, which are of practical interest [70]. The physics can be explained as the efficient screening to the interface traps in FLG with more layers, whereas the difference in the band structures between FLG and SLG also plays a role [66], [70]. In this context, the thickness-graded graphene (GTG) transistor was utilized to study the layer dependence of LFN [64]. The fabrication method was the same as in the conventional back-gated graphene devices. The channel of GTG devices was confirmed to gradually vary from a single-layer in the middle to multilayers (≥ 2 layers) near the source/drain contacts. The measured LFN in GTG and bilayer graphene (BLG) was typically lower than that in SLG with the same device area (S) [see Fig. 3(b)]. The lower LFN in GTG and BLG (than that in SLG) can relate to a smaller metal-doping induced Fermi-level shifts near the contact and/or more effective carrier screening to the interface traps, which result from the difference in their band structures and transport properties [61], [64]. This result shows the layer dependence on the LFN in graphene, providing insight for designing low-noise devices with MLG. The contact engineering is yet another significant aspect in lowering the LFN in graphene devices. However, no consensus about the weight of LFN contribution from the metal–graphene contact (compared to that from the graphene channel) has been reached yet [64], [65], [77], [119]. The results can relate to the fraction

of the contact resistance over the entire device resistance in as-made graphene devices, which depends on the device qualities and the contact material in use [115], [123].

Cleaning the graphene surface is also helpful in lowering the effect of interface traps. The adsorbed particles left on graphene surface during the fabrication, for example, can significantly affect the device performance [129]–[131]. Xu *et al.* [60] have reported an improved LFN level in GNR devices by cleaning the graphene surface. As shown in Fig. 3(c), GNRs were patterned using a Si-nanowire mask to avoid the use of photoresist (e.g., HSQ) which strongly affects device performance [129]. A 20-min, 100 °C vacuum annealing process was conducted to desorb the contaminants on the graphene surface. The cleaned single-layer GNR (SLR) devices feature an improved hysteresis (during a dual sweep of the gate bias) and a 30% lower LFN than those achieved by HSQ-based methods [61]. The LFN improvement can be attributed to a cleaner graphene surface, whereas the four-probe configuration also reduces the noise contributed from the contacts as in two-probe setups. This work presents an approach of achieving low-noise GNR devices using the nanowire-patterning method.

Last, improving the substrate quality can also reduce the number of interface traps in graphene devices. For instance, boron–nitride (BN) substrate shows its potential in achieving high-performance graphene devices, which outweigh those on SiO_2 substrates [3], [40]. Its superior properties, such as ultraflat surface with very few dangling bonds and charge traps, are expected to minimize the trap-induced fluctuations and lower the noise. Suspending graphene (i.e., free of substrate) is another option to greatly reduce the LFN with much fewer traps in devices [119], which may show promise for low-noise applications. A recent study shows that the graphene devices can have 6–12 times lower LFN by etching away the SiO_2 substrate, which can benefit the device performance in pH-sensing applications [118].

Reducing the effect of interface traps is a key issue to continued miniaturization of graphene devices, circuits, and systems. Future studies require the clear understanding of their physical mechanisms and a systematic optimization of the device engineering.

IV. EDGE DISORDER: GRAPHENE VARIABILITIES FROM MATERIAL IMPERFECTION

Unlike a CNT with a perfectly enclosed structure, graphene usually has unavoidable edge disorders for its planar geometry [12]. As the width of graphene narrows down to the nanometer scale, a graphene nanoribbon (GNR) would become very sensitive to the scattering induced by these edge disorders [5]. One should also mention that the edge disorder produces a major detrimental effect on the graphene thermal conductivity [132]–[135]. The question of how to control the edge disorders in GNR devices well is essential in evaluating the graphene scaling along the width direction and the practicality of GNR electronics: GNR has an energy gap that benefits the device switching; however, its mobility can be seriously degraded by edge disorders [1], [5]. We next discuss their concepts, roles on device performance, and the ways of reducing their impact by improving the material quality.

A. Type of Edge Disorders

Various edge disorders exist in as-made GNR devices [91]. It is important to identify the difference in their origin, morphology, and length scale. Here, we discuss the main categories of edge disorders that are commonly referred to in the literature (see Fig. 4).

1) Carbon atoms (C-atom) form dangling bonds at the GNR edge, which can bind to different atoms, including H, O, F, and OH [see Fig. 4(a)] [136]. Due to the difference between the local density of states at the edge and that in the center of the GNR, these edge disorders serve as scattering sites. This type of edge disorders can even exist in GNRs with perfect zigzag or armchair edges.
2) Mixed edge structure composed of both zigzag and armchair edges are broadly observed in as-made GNRs [see Fig. 4(b)] [12], [137], whereas edge structures beyond zigzag and armchair edges are also reported [138]. The existence of these edge disorders partly explains why the chirality dependence of GNR can be diluted in real samples [139], which do not follow the theoretical predictions based on pure zigzag or armchair edges.
3) C-atoms at the edge can restructure themselves into other morphologies [see Fig. 4(c)]. These edge disorders can be in the form of dislocations within or out of the GNR plane [91], [140]. Examples include point defect, vacancies, 5-7-5 or 5-8-5 edge deformations, loops, line defects, adatoms, and interstitials. Study of this type of edge disorders is at its early stage.
4) Multilayer GNRs can form a partially closed edge structure [see Fig. 4(d)]. This type of edge disorders has been found in both GNRs and micron-wide graphene sheets [141]–[143]. They may weaken the edge-induced carrier localization in multilayer GNRs compared to that in SLRs [144], since the carriers can couple among different layers through the closed edges.
5) Line edge roughness (LER) and line-width roughness (LWR) also exist in as-made GNRs [see Fig. 4(e)]. Depending on the material preparations, LER/LWR can have a length scale of 10^0–10^1 nm, which is directly observable using atomic force microscopy (AFM) [59]. If LER/LWR becomes serious, GNR behaves more like a chain of connected quantum dots and forms a Coulomb blockade [145]. LER/LWR is expected to be more

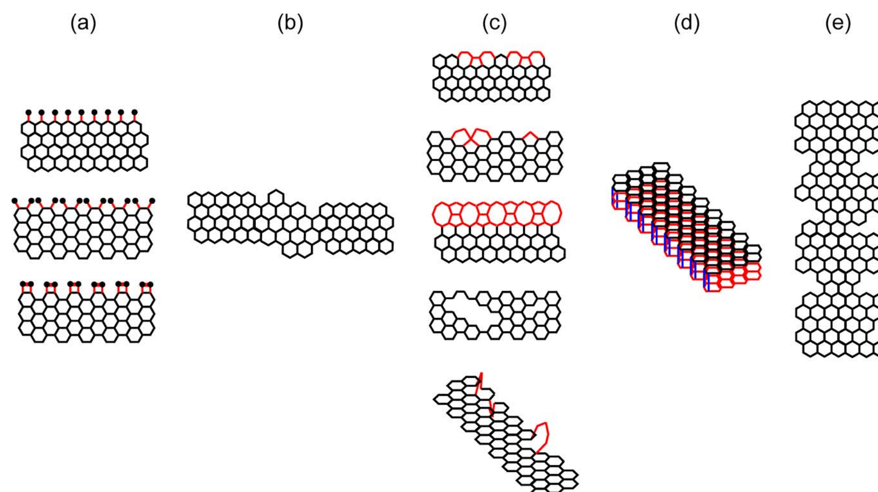

Fig. 4. *Main categories of edge disorders in as-made GNR/graphene materials. (a) The dangling bonds of the outmost C-atoms can bind to H/F/OH/O atoms (in red) [136], which even exist near the perfect zigzag (top panel) or armchair edges (middle and bottom panels). The top and middle panels show typical H or F atoms near the GNR edge, where the bottom panel shows typical O atoms near the GNR edge. (b) Mixed edge structure composed of both zigzag and armchair edges [12], [137]. (c) Restructured C-atoms near the edge (in red) [91], [140]. Examples are illustrated from top to bottom: (in-plane) 5-7-5 dislocations near a zigzag edge, 5-7-5 dislocations near an armchair edge, 5-8-5 dislocations near a zigzag edge, single/multiple vacancies, (out-of-plane) adatoms/interstitials. (d) Enclosed edges (in blue) in BLG or MLG families (number of layers > 2) [141]–[143]. Note that the blue part is just for illustration; C-atoms from different layers may not connect this way. (e) LER/LWR [59]. They have a spatial size of $10^0 \sim 10^1$ nm in the nanowire-mask-based GNR devices.*

controllable by material engineering than the edge disorders with an atomic scale.

Overall, the edge disorders in 1)–3) can be treated as local disturbances (short-range scatters) near the GNR edge; those in 4) and 5) relate to the irregularities that deviate from ideal GNRs [91], [140]. Whichever categorizations we take, it is clear that the component of edge disorders in GNR (and graphene sheet) is complicated. Due to the lack of accurate manipulation of these edge disorders, most experiments could not differentiate the role of a certain type of edge disorders from the others at the moment. The solution can appear with the advancement of fabrication and characterization methods.

B. Effects of Edge Disorders on Device Performance

Edge disorders in as-made GNRs raise the concern of their impact on transport properties and device operations. For example, the transport gap observed in GNRs makes them advantageous in switching ON/OFF the devices, while the question of how the edge disorders affect or contribute to the observed gap in GNR devices is still debated [130], [146], [147]. Han *et al.* [130] have reported the size dependence of SLR at low carrier densities, attributing the transport gap to a combination of the edge effect and the Coulomb charging effect. However, their fabrication method leaves chemical residues (HSQ) on top of the GNR samples, which makes it difficult to probe the intrinsic GNR properties [139]. In contrast, a study of SLRs prepared by a metal-mask etching method suggests that the transport gap mainly originates from the effect of charged impurities instead of edge disorders [147]. Given the sensitivity of GNRs to the weight of various scatterings, it may not be surprising to see the inconsistency of the role of edge effects in these measurements, since SLR devices fabricated through different methods can yield quite different transport properties (see details in Table 3) [13], [14], [60], [129], [139], [147]–[157]. Details in sample preparations can affect the weight of edge-induced scattering in specific GNRs, and need to be considered for comparing the results. On the other hand, Yang and Murali [150] have studied the width dependence of carrier mobilities in GNR-array devices patterned by lithography. The decrease of mobility in samples with a narrower width was attributed to the increased scattering from LER, which poses a constraint to the device performance.

Xu *et al.* [58] have recently employed the length dependence of sample resistance (i.e., resistance scaling, R–L relation) to investigate the role of edge disorders in the transport of SLG and BLG and GNR (SLR and BLR) devices (see Fig. 5). According to one-parameter scaling law, R–L relation can identify the transport regimes in low-dimensional systems, such as the exponential R–L relation and linear the R–L relation for localization and diffusion regimes, respectively [81], [158], [159]. Here, GNRs were fabricated by a nanowire-mask etching method with good performance, as reported before [60]. The room-temperature sample resistance was measured within the low-bias regime at both low and high carrier densities. The experimental data showed that the SLR transport lies in a strong localization regime (exponential R–L relation),

Table 3 Typical Fabrication Methods of GNR Devices. Plasma-Based GNR Fabrication Methods Typically Use O_2/Ar Plasma Etching to Form the GNR, With Chemical Resists, Nanowires or Metal Lines Being Employed as the Etching Mask [14], [60], [129], [139], [147]–[157]. On the Other Hand, GNRs Can Be Chemically Derived via Unzipping CNTs [152], [153] or Thermally Grown on SiC Wafers [13]. The Chemical-Solution-Based Method Can Achieve Ultranarrow GNRs With a Sub-5-nm Width [152]. Since GNR Is Sensitive to Multiple Types of Scattering, It May Not Be Surprising to See the Inconsistency in Their Transport Properties, Which Can Be Quite Different in Samples Prepared by Different Methods. HSQ and PMMA Are the Photoresist Materials Used in Ebeam Lithography

Data source	Contact	GNR preparation	GNR surface
M. Y. Han [139]	Cr/Au	HSQ mask + O_2 plasma	HSQ coverage
Y. M. Lin [129]	Pd	HSQ mask + O_2 plasma	HSQ removed by HF
C. Lian [148]	Cr/Au	Al mask + O_2 plasma	Al removed by etchant
P. Gallagher [147]	Ti/Au	Ti mask + O_2 plasma	Ti and PMMA removed
J. Bai [149]	Ti/Au	Si nanowire mask + O_2 plasma	Si nanowire coverage
Y. Yang [150]	Ti/Au	HSQ mask + O_2 plasma	HSQ coverage
Z. Chen [151]	Pd	HSQ mask + O_2 plasma	HSQ removed by HF
L. Jiao [152]	Pd	gas phase oxidation + sonication	GNR formed by unzipped CNT
L. Jiao [153]	Pd	PMMA protection + Ar plasma	GNR formed by unzipped CNT + PMMA removed
G. Xu [60]	Ti/Au	Si nanowire mask + O_2 plasma	Si nanowire removed
M. Sprinkle [13]	Pd/Au	SiC growth on $(1\bar{1}0n)$ facet (n~8)	GNR formed by SiC
R. Yang [154]	Ti/Au	PMMA mask + O_2 plasma + H_2 plasma etching	PMMA removed
X. Wang [155]	Pd	Al mask + Ar plasma + $(NH_3 + O_2)$ etching	Al removed by etchant
X. Li and X. Wang [14]	Pd	Chemically-derived from solution	GNR dispersed on substrate
D. V. Kosynkin [156]	Pt	Chemically-derived from solution	GNR formed by unzipped CNT
J.B. Oostinga [157]	Ti/Au	PMMA mask + Ar plasma	PMMA removed

which can be attributed to a strong edge effect [see Fig. 5(a)]. In contrast, BLRs featured diffusive transport (linear R–L relation), where the absence of localization can relate to a weaker edge effect than that in SLRs [see Fig. 5(b)]. Through the comparisons among SLR, BLR, SLG, and BLG, the edge effect in graphene materials was found to be reduced by enlarging the width, decreasing the carrier densities, or adding an extra layer [see Fig. 5(c)]. From SLR to SLG, the data showed a dimensional crossover of the transport regimes possibly due to the drastic change of the edge effect. These results reveal a critical role of edge effect in graphene transport and thus the resistance scaling rules, which may provide insight to achieve scalable graphene electronics.

Another recent work has reported a direct analysis of the LWR in GNR devices fabricated by the nanowire-mask method [59], [160]. The edge profile of GNRs was extracted from their AFM/SEM images by an image processing algorithm [see Fig. 6(a)]. Then, the width values were sampled along the L-direction of the edge-profile image, which were used to calculate the standard deviation (σ) as the LWR amplitude. The LWR amplitude among 13 SLRs and five BLRs was found to generally decrease with the GNR width (W), and the smallest LWR amplitude was below 5 nm for SLRs with $W \sim 30$ nm [59]. This result can relate to the etching undercut due to the circular cross section of the nanowire mask. The W-dependence of ON/OFF ratios in the GNRs with different σ values was measured to evaluate the LWR impact on device performance (see Fig. 6(b); the $G_{\text{on}}/G_{\text{off}}$ ratio at $T = 300$ K is calculated by the measured conductance (G) at $|V_g - V_{\text{Dirac}}| = 30$ V and $V_g = V_{\text{Dirac}}$, respectively). The data showed a large variation in the W-dependence of the $G_{\text{on}}/G_{\text{off}}$ (e.g., the $G_{\text{on}}/G_{\text{off}}$ value in SLRs varies from 2.2 to 3.5 near $W \sim 40$ nm), with

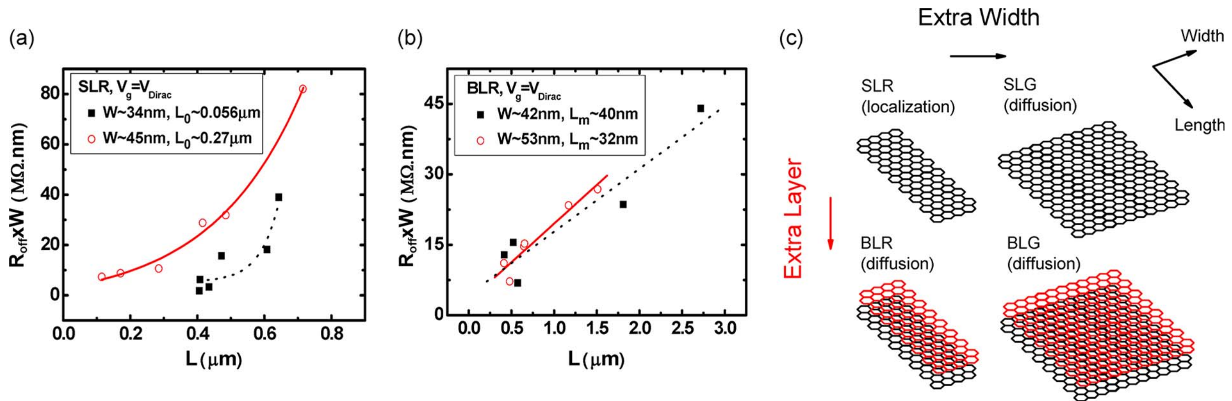

Fig. 5. *Effect of edge disorders on resistance scaling rules in graphene nanostructures [58]. (a) Room-temperature $R-L$ relations for SLR at off-state ($V_g = V_{\rm Dirac}$), where $R_{\rm off}$ exponentially increases with L. The fitting showed a characteristic localization length of $L_0 \sim 0.27$ μm for $W \sim 45$ nm and $L_0 \sim 0.056$ μm for $W \sim 34$ nm, respectively. (b) Room-temperature $R-L$ relations for BLR at off-state ($V_g = V_{\rm Dirac}$), where $R_{\rm off}$ linearly increases with L. The fitting showed a characteristic mean-free path of $L_m \sim 40$ nm for $W \sim 42$ nm and $L_m \sim 32$ nm for $W \sim 53$ nm. (c) Schematics for the crossover of transport regimes in graphene devices. This edge effect in SLR can be weakened by either adding an extra layer to form BLR or increasing the width to form SLG; both cause the transition of transport regimes from localization to diffusion.*

no clear dependence on the σ values. This large variation of ON/OFF ratios in GNRs in the presence of LWR is consistent with theoretical works [161]–[163]; however, it may not be fully attributed to LWR because other atomic-scale edge disorders can also contribute to the variations. Although LWR itself could lead to device degradation, the complexity in the component of edge disorders needs to be taken under account in as-made GNRs.

C. Advancement in Reducing Edge Disorders in Graphene

Edge disorders represent the graphene variabilities posed by material preparations, which challenge the reliability and scalability of graphene systems. Much progress has been made to reduce their effect through the advances of material synthesis and patterning methods, with some technology showing very promising results (see details in Table 3). For example, Wang *et al.* have developed a gas phase etching chemistry to narrow the GNRs down to < 10 nm with a well-controlled etching rate [155]. The achieved sub-5-nm-wide GNR devices show a high ON/OFF ratio up to $\sim 10^4$ at room temperature. On the other hand, Jiao *et al.* [153] have demonstrated high-performance GNRs derived from unzipping multiwalled CNT samples. They achieve this by either plasma etching of the CNTs in a polymer film, or mechanical sonication of the gas-phase oxidized CNTs in an organic solvent. The obtained GNR devices have very smooth edges and the room-temperature mobility as high as 1500 $\text{cm}^2/(Vs)$ with a 10–20-nm width. A recent study shows that these GNRs can behave as perfect quantum wires under low temperature [15]. Moreover, Cai *et al.* [164] reported an atomically precise bottom-up fabrication of GNRs, which can provide GNRs with engineered chemical and electrical properties. The

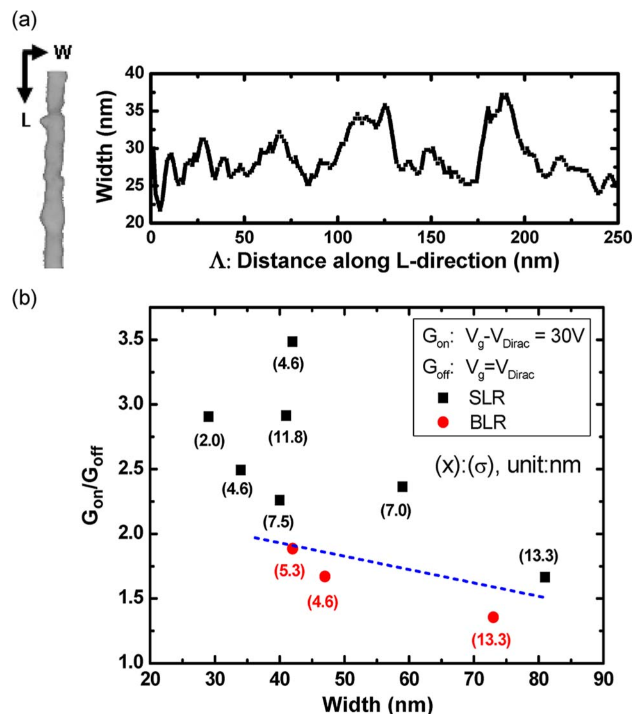

Fig. 6. *LWR analysis for GNRs [59]. (a) Left panel: The extracted GNR edge profile from the AFM image for LWR analysis. Right panel: The width sampling (smoothened) along the L-direction of an SLR versus the distance along the L-direction (Λ). The LWR amplitude σ was defined as the standard deviation of the sampled width values. (b) The ON/OFF ratios ($G_{\rm on}/G_{\rm off}$) of as-made GNRs (both SLRs and BLRs, $T =$ 300 K) versus the averaged width (W). The low-bias conductances ($G_{\rm on}/G_{\rm off}$) at both ON- and OFF-states were measured at $V_g - V_{\rm Dirac} = 30$ V and $V_g = V_{\rm Dirac}$, respectively. The values of σ were labeled at each data point (unit: nanometers). The guide to the eye showed that the ON/OFF ratios are generally lower in BLRs than those in SLRs.*

topology, width, and edge profile of GNRs are well defined by the structure of the precursor monomers, which are prepared by surface-assisted coupling and cyclodehydrogenation. This work provides another approach in developing high-performance GNR devices. Overall, we expect that the continuous technology improvement with an accurate manipulation of the edge disorders will bring much more excitement in graphene community.

V. GRAPHENE VARIABILITIES FOR SENSING APPLICATIONS

While variabilities in graphene are generally considered the challenges for device engineering, a revisit of their concepts can open up potential applications. Recent studies have revealed strong correlations between the "signal fluctuations" in graphene devices with their surrounding environment and the material properties (e.g., band structures) [65], [71], [75], [76]. By characterizing the graphene variabilities (e.g., LFN), one can thus probe the environmental change near the graphene surface and the alteration of graphene properties. This variability-based probing mechanism, although at an early stage of development, can be useful in graphene-based sensing applications. Similar ideas have been implemented in silicon-nanowire and carbon nanotube devices, where the LFN can be employed in gas sensing and biosensing with high sensitivities [82], [165].

For example, charged impurities left near the graphene–SiO_2 interface can create an inhomogeneous charge distribution along the graphene sheet, which is a dominating scattering mechanism that limits the carrier mobility and can be responsible for several physical anomalies near the Dirac point [see Fig. 7(a)] [5], [87], [88], [166], [167]. To investigate how the presence of spatial charge inhomogeneity influences the LFN behavior in graphene, Xu *et al.* [65] conducted research on the gate dependence of the LFN amplitude (A) in back-gated SLG and BLG devices built on a SiO_2/Si substrate. Graphene devices were maintained in a vacuum environment and a 20-min vacuum bakeout (100 °C) process was generally applied before the LFN measurements. Using a four-probe measurement (4T) setup as described before (see Section II), the gate dependence of LFN in SLG and BLG was found to feature an M-shape and V-shape, respectively [see Fig. 7(b) and (c)]. The analysis showed that the noise behavior near the Dirac point can be attributed to the extent of spatial charge inhomogeneity at low carrier density limits (e.g., the noise maximum in the M-shape of SLG matches the density of charged impurities n_{imp}). The correlation between the gate dependence of LFN and the spatial charge inhomogeneity in graphene can act as a probing mechanism to characterize the nonuniform doping profile of graphene. For instance, the LFN spectroscopy indicates the amount of charged impurities near the graphene surface, which can be used

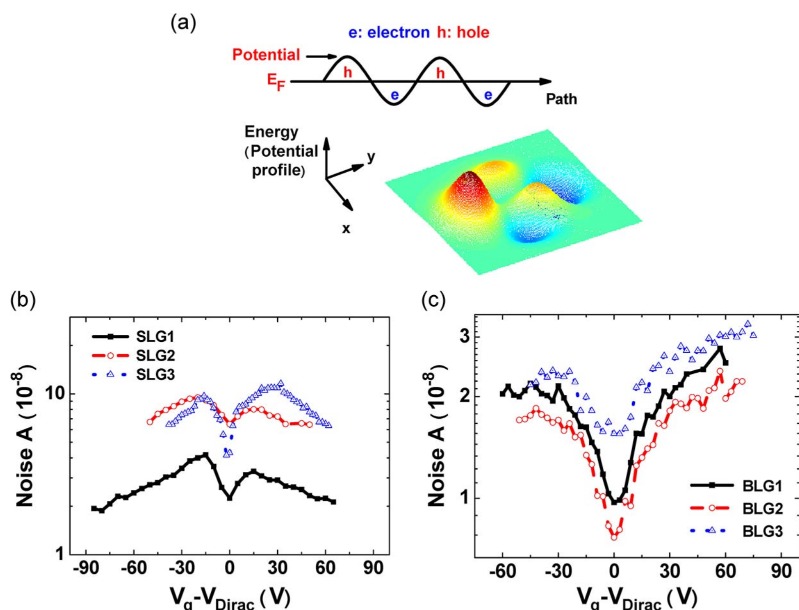

Fig. 7. ***Gate dependence of LFN in graphene devices: Probing the charge impurities by noise behavior [65]. (a) Charged impurities near the graphene–SiO_2 interface can create an inhomogeneous charge distribution along the graphene sheet, which is a dominating scattering mechanism that limits the carrier mobility. (b) Gate dependence of LFN amplitude (A) in SLG featured an M-shape at room temperature (shifted by the gate bias at the Dirac point V_{Dirac}). (c) Gate dependence of LFN amplitude (A) in BLG featured a V-shape at room temperature (shifted by V_{Dirac}). The analysis showed that the noise behavior near the Dirac point can be correlated to the extent of spatial charge inhomogeneity at low carrier density limits (e.g., the noise maximum in the M-shape of SLG matches the density of charged impurity n_{imp}).***

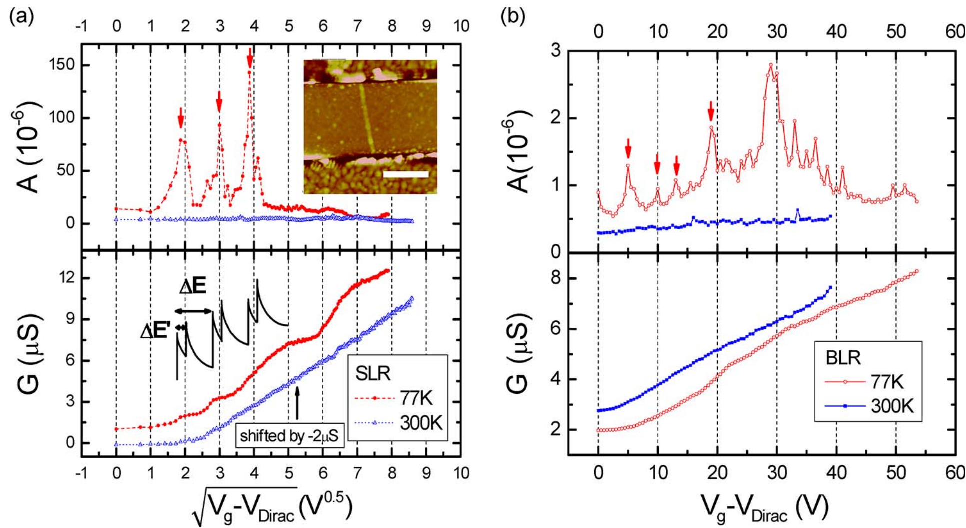

Fig. 8. *Gate dependence of LFN in GNR devices: Probing the band structure by noise behavior [71]. (a) Temperature-dependent noise (A, top) and conductance (G, bottom) in SLR ($W \sim 42$ nm, $L \sim 0.81$ μm) in the scale of $\sqrt{V_g - V_{\rm Dirac}}$ for the electron–conduction side ($V_g > V_{\rm Dirac}$). The upper inset shows the AFM image of the SLR device with a scale bar equal to 0.5 μm. At 77 K, the gate dependence of LFN showed peaks whose positions quantitatively matched the subband positions in the quasi-1-D DOS (see the lower inset for the schematics). The strong correlation between LFN and DOS provides a robust mechanism to electrically probe the band structure of GNRs. (b) Temperature dependence of LFN behavior in BLR ($W \sim 49$ nm, $L \sim 0.79$ μm) was presented in scale of $V_g - V_{\rm Dirac}$ for the electron–conduction side ($V_g > V_{\rm Dirac}$). At $T = 77$ K, the noise peaks (as arrowed) appeared while the corresponding conductance plateaus (bottom) were not obvious.*

to evaluate the substrate/dielectric quality of graphene devices.

Taking one step further, Xu *et al.* [71] extended the LFN study in back-gated SLR and BLR devices, aiming to investigate the impact of their quasi-1-D transport on the noise behavior. The GNR devices were achieved by the nanowire-mask-based method [see the inset of Fig. 8(a)], and kept in vacuum for both LFN and dc conductance measurements. Data were presented in the energy scale to compare with the band structure ($\sqrt{|V_g - V_{\rm Dirac}|}$ in SLR; $|V_g - V_{\rm Dirac}|$ in BLR). Through the analysis, the enhanced conductance fluctuations (noise) were found to originate from the quantum confinement along the GNR widths. In SLRs, the gate dependence of LFN showed peaks whose positions quantitatively match the subband positions in the quasi-1-D band structures (see Fig. 8(a); $W \sim 42$ nm). The LFN peaks can be attributed to the enhanced trap-induced conductance fluctuation: the fluctuating occupancy of interface traps causes the variation of the local potential; the resulting conductance fluctuation is enhanced near the subband thresholds where the density of states (DOS) diverges [71], [79]. In BLRs, the LFN peaks were also obvious while the subband feature was unclear in conductance data (see Fig. 8(b); $W \sim 49$ nm). Overall, the correlation between LFN and DOS provides a more robust mechanism to electrically probe the band structure of GNRs than the conductance measurement (where the subband feature is not clearly seen from the conductance plateaus). High-quality GNRs with a narrower width (e.g., sub-10 nm) are expected to result in a larger separation among the noise peaks and larger noise amplitudes (for a smaller GNR area), which would make the noise peaks observable at 300 K or higher temperatures. The gate dependence of LFN can be employed to probe the change of GNR band structures, which can find its use in a broad range of sensing applications. For example, the LFN spectroscopy of GNR can detect the surface functionalization, the biomolecule attachment, and the strain variations, all of which alter the band structure of GNRs chemically, biologically, or mechanically.

A recent study by Rumyanttsev *et al.* [75] has demonstrated the LFN-based selective gas sensing in back-gated graphene device. The room-temperature LFN spectra were collected in 1 min after the device exposure to the chemical vapors with a well-controlled pressure (a degassing process was applied before switching the vapors). The data showed a discernible change of the LFN spectra due to the graphene exposure to chemical vapors [see Fig. 9(a)]. The noise spectra in open air were close to the 1/f shape, whereas most vapors introduced Lorentzian bulges over the 1/f noise background. The Lorentzian noise components can relate to the additional traps created by the gas molecules, which lead to the trapping/detrapping processes with specific time constants [104]–[108]. Furthermore, the normalized LFN multiplied by frequency ($S_I/I^2 \times f$) featured a maximum at a characteristic frequency f_c [see Fig. 9(b)], which was different in different vapors (e.g., $f_c \sim$ 10–20 Hz and 500–700 Hz for tetrahydrofuran and acetonitrile, respectively). The LFN spectra were reproducible from multiple measurements, which can be

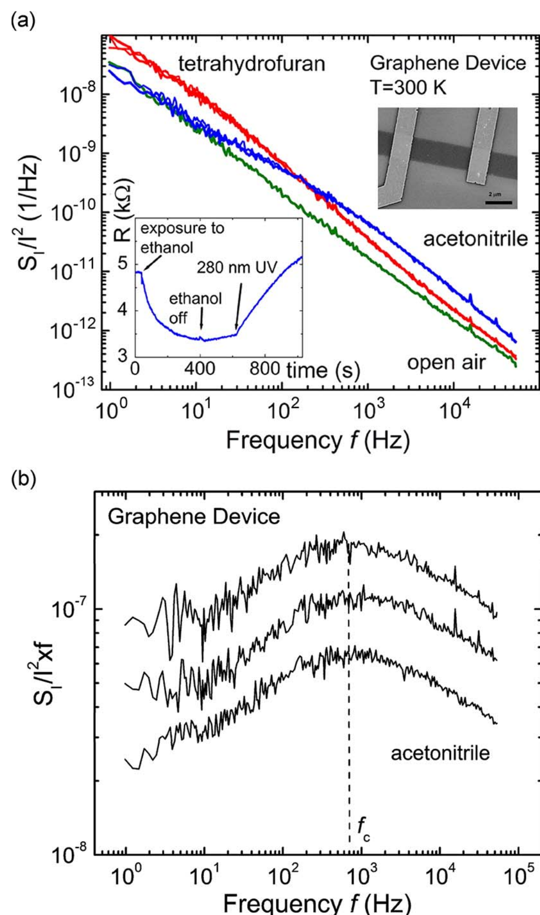

Fig. 9. ***Selective gas sensing in back-gated graphene devices [75]. (a) LFN spectra of SLG devices measured in open air and under the exposure to acetonitrile and tetrohydrofuran vapors ($T = 300$ K at $V_g = 0$ V). The source-drain voltage is biased at $V_{ds} = 100$ mV. The left inset shows the real-time resistance response of a graphene device ($V_g = 0$ V) to the exposure of ethanol. The right inset shows the typical scanning electron microscopy (SEM) images of a back-gated graphene device with a scale bar equal to 2 μm. (b) Normalized LFN spectra multiplied by frequency ($S_I/I^2 \times f$) in three SLG devices exposed to acetonitrile vapor. All three devices feature the same characteristic frequency f_c, showing excellent reproducibility of the noise response to chemical gases.***

used for reliable chemical sensing. The frequency f_c of vapor-induced noise spectra, in combination with the real-time resistance changes [see the left inset of Fig. 9(a)], can serve as distinctive signatures for highly selective gas sensing by a single graphene device. This approach avoids the fabrication of a dense sensor array which requires specific functionalization for individual gases.

The idea of LFN-based metrology has also been implemented on the scanning probe microscopy (SPM) platform. Sung *et al.* [76] have recently developed a scanning noise microscopy (SNM) for graphene strip devices: a scanning Pt tip is contacted to the graphene surface to measure the current noise spectrum through it. The length dependence of the LFN amplitude was analyzed using an empirical model, which extracted the noise contribution from the device channel. Importantly, this SPM method gave a 2-D noise mapping of the graphene strip device, which clearly indicated the spatial fluctuations of the graphene qualities (e.g., structural defects). The SNM method can be integrated in existing SPM technologies and achieve a spatial resolution as small as 1 nm by optimizing the tip size. A high-resolution noise mapping can be useful in detecting the local surface qualities on graphene and many other materials, which can benefit fundamental research on nanoscale devices.

The development of variability-based sensing applications with graphene can bring research opportunities in multiple fields. For example, if a single-trap graphene system can be achieved, the statistical analysis of RTN can be employed to extract the trap information. For example, the spatial location of a single trap away from the graphene surface can be estimated by the gate dependence of the time constant ratios (i.e., τ_1/τ_2) [111]. And the RTN behavior under a magnetic field can detect the spin resonance of a single electron in graphene devices, which may provide interest for graphene spintronics [168]. The new role of graphene variabilities, employing the "signal fluctuations" as the "sensing signal," would attract both fundamental and practical interest.

VI. CONCLUSION

This paper has reviewed the variability effects in graphene, with emphasis on their challenge and opportunities for device engineering and applications. The variabilities in as-made graphene devices can result from the environmental disturbance (class I) and the material imperfection (class II). In class I variabilities, we review the research on interface traps near the graphene surface, with the focus on their physical principles, characterization methods, and the approach to minimize their effect via device engineering. In class II variabilities, we review the research on edge disorders that broadly exist in graphene materials, discussing their concepts, critical roles in device performance, and the technology advancement in reducing their effect. From the metrology perspective, we discuss the potential use of graphene variabilities for sensing applications, such as the surface-quality detection, selective gas sensing, and SPM technologies, which may promote interest in developing variability-based graphene applications.

Aligning the concepts of graphene variabilities with those in silicon devices, we see that the research is still at an early stage. Efforts need to be made in larger spatial scales with discussions from the circuit and system perspectives. Even within the device level, an exclusive coverage of this rapidly growing field is difficult for its multidisciplinary nature. For example, structural defects (away from the edges) are important variabilities in bulk

graphene (with a micrometer width), which are much concerned in graphene samples prepared by CVD-based transfer technology [92], [140]. Artificially generated structural defects (e.g., ion irradiation) have been found to lower the mobility, shift the Dirac point, increase the noise, and modify the transport properties [69], [169]–[171]. However, the quality of CVD graphene has been significantly improved in recent years [17], [23], [172]. The effects of structural defects on the performance of CVD-based graphene devices would need to be evaluated with consideration to the presence of other variabilities (e.g., charged impurities). In addition, large geometrical distortions in graphene, such as ripples, can be potentially implemented in strain and thermal engineering [85], [93]. A recent study reveals that a giant pseudomagnetic field (300 Tesla) can be achieved in graphene nanobubbles via strain engineering [173].

With the presence of variabilities, scalability of the graphene devices is a critical issue to evaluate their ultimate promise. Besides the resistance scaling as discussed before (Section III), scaling behaviors of the graphene devices, such as ON/OFF ratio and transconductance, require continuous focus. For example, Sui *et al.* [66] have reported the role of disorder (e.g., charged impurities) to the size scaling of minimum conductivity at Dirac point in SLG devices. Meric *et al.* [174] have characterized the length dependence of the high-bias transport in dual-gated graphene devices, which reveal the effect of interface traps to the output conductance and current saturation. How these graphene variabilities will be affected by size scaling is yet another important topic to investigate. Similar to silicon devices [99], [101], the scaling of graphene devices may increase the impact of graphene variabilities on device performance. As the device scales down, the variabilities with a small scale (e.g., interface traps, atomic-scale edge disorders) might become more influential than those with a large scale (e.g., ripples larger than 300 nm can be less likely to exist in small devices [93]). The effect of graphene variabilities also depends on technology advances. For instance, the scattering rate due to charged impurities is lower in graphene devices on a BN substrate than those on a Si/SiO_2 substrate[3]. Research on these aspects will help the exploration of the scaling limit in graphene electronics.

We finally mark that our discussions can extend to other thin-film, nanowire, and nanotube devices, in all of which variabilities exist and need to be addressed for device applications. A controlled manipulation of these variabilities may lead to flexible metrology tools that can provide surprises in the future. ■

Acknowledgment

The authors would like to thank C. M. Torres, Jr., J. Bai, L. Liao, Y. Huang, M. Wang, E. B. Song, J. Tang, C. Zeng, S. Aloni, T. Kuykendall, F. Liu, F. Miao, X. Zhang, M. Y. Han, E. Rossi, S. Adam, and E. H. Hwang for many stimulating discussions and technical supports.

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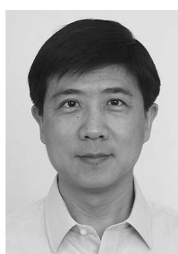

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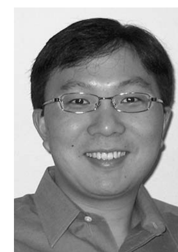

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