Evidence for a thermally driven charge-density-wave transition in 1T-TaS$_2$ thin-film devices: Prospects for GHz switching speed ⓔⓟ

ⓘⒹ Amirmahdi Mohammadzadeh, ⓘⒹ Saba Baraghani, ⓘⒹ Shenchu Yin, ⓘⒹ Fariborz Kargar, ⓘⒹ Jonathan P. Bird, and
ⓘⒹ Alexander A. Balandin

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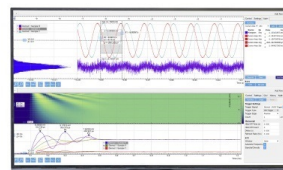ⓔⓟ This paper was selected as an Editor's Pick

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Evidence for a thermally driven charge-density-wave transition in 1T-TaS₂ thin-film devices: Prospects for GHz switching speed

Amirmahdi Mohammadzadeh,[1] (iD) Saba Baraghani,[1] (iD) Shenchu Yin,[2] (iD) Fariborz Kargar,[1] (iD) Jonathan P. Bird,[2] (iD) and Alexander A. Balandin[1,a)] (iD)

AFFILIATIONS

[1]Nano-Device Laboratory (NDL) and Phonon Optimized Engineered Materials (POEM) Center, Department of Electrical and Computer Engineering, University of California, Riverside, California 92521, USA

[2]Department of Electrical Engineering, University at Buffalo, The State University of New York, Buffalo, New York 14260, USA

Note: This paper is part of the APL Special Collection on Charge-Density-Wave Quantum Materials and Devices.
a)Author to whom correspondence should be addressed: balandin@ece.ucr.edu. **URL:** http://balandingroup.ucr.edu/

ABSTRACT

We report on the room-temperature switching of 1T-TaS₂ thin-film charge-density-wave devices, using nanosecond-duration electrical pulsing to construct their time-resolved current–voltage characteristics. The switching action is based upon the nearly commensurate to incommensurate charge-density-wave phase transition in this material, which has a characteristic temperature of 350 K at thermal equilibrium. For sufficiently short pulses, with rise times in the nanosecond range, self-heating of the devices is suppressed, and their current–voltage characteristics are weakly nonlinear and free of hysteresis. This changes as the pulse duration is increased to ∼200 ns, where the current develops pronounced hysteresis that evolves nonmonotonically with the pulse duration. By combining the results of our experiments with a numerical analysis of transient heat diffusion in these devices, we clearly reveal the thermal origins of their switching. In spite of this thermal character, our modeling suggests that suitable reduction of the size of these devices should allow their operation at GHz frequencies.

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Charge-density wave (CDW) phenomena have recently witnessed renewed interest, particularly in the context of two-dimensional (2D) van der Waals materials.[1–8] This interest is driven by both exciting physics and possible practical applications that can be derived from such materials. CDW transitions can be induced by various perturbations, including heating,[9] doping,[10–14] electrical pulsing,[15–17] substrate effects,[18] gate biasing,[17,19,20] and alteration of the thickness of the material.[21–23] The 1T polymorph of TaS₂ is one of the 2D van der Waals materials of the transition-metal dichalcogenide (TMD) group that reveals phase transitions in the form of abrupt resistivity changes and hysteresis.[24,25] Since two of these transitions are above room temperature (RT), 1T-TaS₂ has attracted attention for applications, such as high-speed memory devices,[17] oscillators,[20,26,27] transistor-less logic circuits,[28] oscillatory neural networks,[29] and logic gates.[30–32] The fact that two-terminal devices implemented with 1T-TaS₂ are radiation hard is an additional benefit.[26,33]

The resistivity changes exhibited by several TMDs, e.g., 1T-TaS₂ and 1T-TaSe₂, are attributed to transitions among different CDW phases.[24] The CDW phase is defined as a periodic modulation of the electronic charge density, accompanied by distortions in the underlying crystal lattice, and may be commensurate or incommensurate (IC) with the underlying crystal lattice.[10,16,24,34–40] The commensurate CDW (C-CDW) phase is typically observed at low temperature. It exhibits a stronger charge density distortion, and it is often pinned to the lattice.[41,42] The C-CDW phase only appears if the thickness of the films is sufficiently large. The lattice distortion in the C-CDW phase forms aggregates of 13 Ta atoms in the shape of a star in the basal plane, with 12 atoms at the vertices of the star inclines and 1 atom at its center.[43–47] From 180 K to 350 K, the aggregates partially melt, forming separate star-shaped islands that represent the nearly commensurate CDW (NC-CDW) phase. Increasing the temperature beyond 350 K, all the aggregate islands melt, and an incommensurate CDW (IC-CDW) phase emerges. Finally, the transition to the normal metallic phase (NP) happens in the range of 500–600 K.[17,20,24,34,35,48–56] The transition temperature between the NC and IC-CDW phases—at 350 K, conveniently above RT—makes 1T-TaS₂ particularly promising

for device applications. The transition temperature is normally determined from transport measurements, in which the temperature of the sample is controlled externally while the electric bias is kept low to avoid local Joule heating.[57] While switching with the bias can pave the way to new electronic devices, different from conventional transistors, there are unanswered questions regarding the mechanism of the phase transitions in 2D CDW materials and devices.

In principle, at least, the application of an electric field can trigger the CDW phase transition directly by affecting the charged ions and electrons in the crystal. If CDW-device operation relies on depinning of the CDW from defects, the electric field can set the CDW in motion above a certain threshold field.[58,59] Alternatively, however, the electric current induced by the field is responsible for Joule heating, which, in turn, can also trigger CDW phase transitions. The strength of the Joule heating should depend on details of the specific material, the device structure, and bias mode (DC vs pulse) and duration. For these reasons, the mechanism of the different phase transitions that arise in different devices is still the subject of debate.[54,60–62] We have previously argued that, in 1T-TaS$_2$ devices on Si/SiO$_2$ substrates, the switching among different CDW phases that is caused by the application of an electric bias results from local Joule heating.[57] This conclusion was reached for devices for which the switching speeds were relatively slow, i.e., in the range of milliseconds to seconds. A recent study, on the other hand, which measured 1T-TaS$_2$ devices with electric pulses of duration 0.1 s, observed that Joule heating could be mostly inhibited.[50] Other related work, also based upon a pulsing technique, came to a different conclusion, namely, that, even for pulses as short as ~0.1 ms, local Joule heating was not eliminated.[63] Elsewhere, a third possible outcome has also been reported, with the NC-CDW to IC-CDW transition being attributed to the electric-field action while the IC-CDW to NC-CDW transition was attributed to local Joule heating.[56] An extra factor that complicates the separation of field- and heating-driven effects arises from the difficulty of making a direct and accurate measurement of local temperature in the μm-scale channels of CDW devices.

Here, we report the results of an experimental investigation of 1T-TaS$_2$ devices under ultra-short electric pulses, combined with a computational study of heat dissipation in these structures. The 1T-TaS$_2$ CDW devices were fabricated on a highly resistive Si/SiO$_2$ substrate in order to allow for ns-duration electrical pulsing. We find that hysteresis, characteristic of the NC- to IC-CDW phase transition, emerges in the current–voltage characteristics of these devices at pulse durations in excess of ~200 ns and that it exhibits a nonmonotonic dependence with increasing pulse length. The experimentally observed evolution of the hysteresis and our numerical solutions of the heat-diffusion equation indicate that the switching is thermally driven. Despite this thermal nature, however, our modeling also suggests that downscaling of the device dimensions, and fine-tuning of the thermal resistance of the structure, should allow for fast operation of such devices, in the GHz frequency range.

High-quality single-crystal 1T-TaS$_2$ (HQ Graphene Co.) was used as the source material in our studies. Thin films of 1T-TaS$_2$ were mechanically exfoliated and transferred to a highly resistive (1–10 Ω cm) Si/SiO$_2$ substrate (525-/0.3-μm, p-type, <100>) with the help of a transfer system that was built in-house. Uniform rectangular flakes were selected for device fabrication to match the pattern of the required on-chip co-planar waveguide [see Fig. 1(e)]. The signal lines
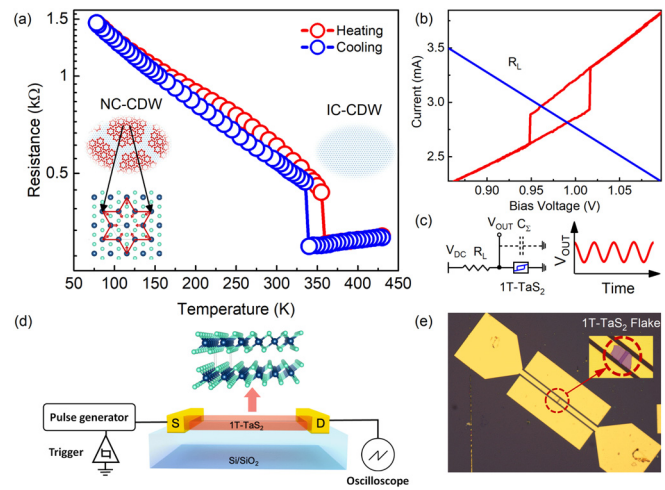

FIG. 1. (a) Temperature-dependent resistance measurement for a thin (<10 nm) 1T-TaS$_2$ film showing the NC- to IC-CDW phase transition at ~350 K. As shown in the insets, the star-shaped islands in NC-CDW phase melt as the temperature rises above 350 K, resulting in the formation of the IC CDW and an accompanying decrease in resistance. (b) The typical current–voltage characteristic of a two-terminal 1T-TaS$_2$ device at RT, exhibiting the hysteresis window and the load line in CDW-based oscillator devices. (c) The left panel is the diagram of a 1T-TaS$_2$ oscillator circuit, including a 1T-TaS$_2$ thin film in series with a load resistor R$_S$ and a lumped capacitance C$_\Sigma$. The right panel shows a schematic of the real-time voltage oscillation generated by such devices. (d) Schematic showing the pulsed-measurement setup. A pulse generator creates repetitive current pulses as short as 8 ns. The generated current is then measured by a mixed-signal oscilloscope. (e) Optical image of the 1T-TaS$_2$ device designed for pulsed measurements. The inset shows a magnified image of the channel with the flake colored in purple for clarity. The gap between the two signal lines was 3 μm.

of this waveguide were 9-μm wide and were separated on either side by 3-μm gaps from two large ground planes, ensuring the 50-Ω matching needed for high-speed measurements. Details of the waveguide structure and measurement setup were reported in Ref. 64. To help preserve this matching, the 1T-TaS$_2$ crystals were chosen to be of the same width as the signal lines. Structures were fabricated by electron-beam lithography and liftoff of Ti/Au (20-/180-nm), deposited by electron-beam evaporation. To avoid degradation of the quasi-2D 1T-TaS$_2$ from exposure to chemicals and air, successive fabrication steps were performed with minimal delay. Fabricated devices were then stored and tested under vacuum conditions.

Figure 1(a) shows the temperature-dependent resistivity of a device implemented with a thin channel (<10 nm) of 1T-TaS$_2$, showing the NC to IC-CDW phase transition at ~350 K. The current–voltage (I–V) characteristics measured for the same 1T-TaS$_2$ device are presented in Fig. 1(b). The straight line is an example of the load-resistance characteristic required to make the oscillator shown schematically in Fig. 1(c). The implementation of such voltage-controlled oscillators from 1T-TaS$_2$ CDW devices has been reported previously by some of us.[20,26] Other fabricated devices had larger thicknesses (~70 nm) to make them more robust for the testing and to ensure contact quality. A schematic of the pulsed-measurement setup is presented in Fig. 1(d). This includes a pulse generator that sources ramped (triangular) current pulses of duration as short as 8 ns and a

mixed-signal oscilloscope (Keysight DSOX6004A, 6 GHz bandwidth) that is used to measure the time-dependent variation of the generated current.

The pulsed measurements were performed in a custom-designed setup with full impedance matching (50 Ω). The device chip was mounted on an FR-4 laminate carrier, which allowed the signal line of the previously mentioned on-chip coplanar waveguide to be connected to the measurement instruments through semirigid coaxial cables and high-bandwidth sub-miniature version A (SMA) connectors. A 50-Ω RuO$_2$ thick film resistor, soldered onto the chip carrier, provided a matched termination for the input signal. An Aim-TTi TGP3151 pulse generator was used to provide the pulses. In this study, repetitive (75 kHz) triangular pulses of various width (8–13 333 ns) were applied to the CDW device input. The resulting output pulses were then captured at the 50-Ω input channel of the oscilloscope and correlated with the input signal to generate a pulsed I–V characteristic. All measurements were performed with the CDW devices mounted inside a customized, light-tight vacuum chamber ($\sim 10^{-6}$ mbar), held at RT.

Figures 2(a)–2(d) show the I–V characteristics obtained for different pulse durations (see the supplementary material, Fig. S1). In all panels, only the I–V results of the first generated pulse are presented. This is essential to eliminate the influence of heat accumulation,

originating from the application of repetitive pulses, on the I–V characteristics of the device. The most important observation is that, when the pulse duration is too short [see Fig. 2(a) with the 8-ns pulse], the I–V curves do not reveal any hysteresis. As the pulse duration is increased, however, the hysteresis, associated with the NC to IC-CDW phase transition, emerges [Fig. 2(b), bias voltage of $\sim$1.65 V]. Visual inspection of the form of the I–V curves in this figure shows that the area associated with the hysteresis increases rather rapidly at first [compare Figs. 2(a) and 2(b)], but then starts to decrease [Figs. 2(c) and 2(d)]. This behavior is attributed to the difference in the time constants for the rate of heat accumulation as a result of Joule heating and the rate of the heat dissipation to the underlying substrate. Overall, these data are consistent with the thermally driven transition scenario; while the maximum strength of the electric field is the same for all of the pulses, the rate of the generated heat in the device and the dissipated heat depend strongly on the pulse duration. More specifically, we suggest that the ultra-short pulses of a few-ns duration are not sufficiently long to increase the local temperature to the vicinity of $\sim$350 K and to thereby drive the NC to IC-CDW phase transition. As the pulse duration is increased, however, heat should accumulate increasingly in the channel, leading to a rise of the local temperature and the emergence of the NC to IC-CDW hysteresis. The further
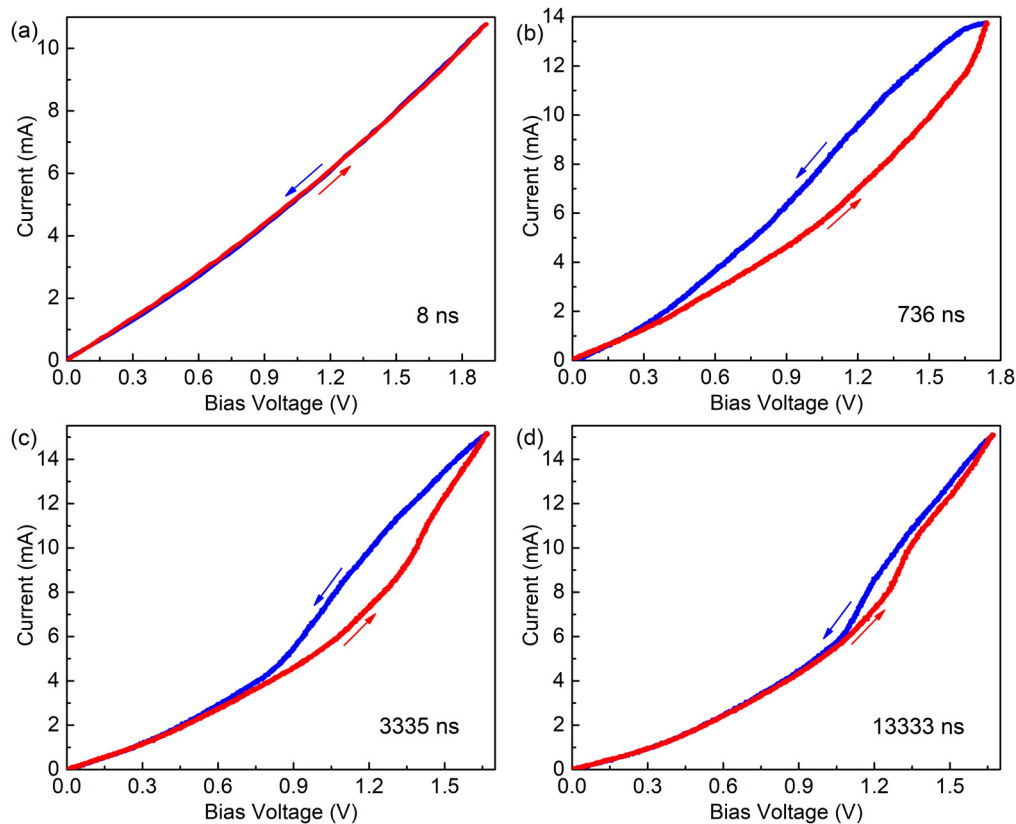

FIG. 2. Experimental current–voltage characteristics, determined using total pulse durations of (a) 8 ns, (b) 736 ns, (c) 3335 ns, and (d) 13 333 ns. For the shortest duration shown (8 ns), no hysteresis window is observed. With increasing the pulse duration, the width of the hysteresis window expands and then shrinks again as the pulse duration approaches to 13 333 ns. This behavior is attributed to the transient heat diffusion characteristics of the 1T-TaS$_2$ film, during the up and down sections of the pulse, causing the film to attain different temperatures at fixed bias in the hysteresis region.

evolution can then be understood as arising from an interplay of two time-constants—one associated with how fast heat accumulates in the channel, and the other with how fast heat escapes from it. These time constants will depend on the pulse duration, the thermal resistance of the device, and its size. When the pulse becomes too long [of μs duration, as in Fig. 2(d)], the local temperature does not decrease sufficiently between pulses to achieve full-size hysteresis, resulting in the decrease in the hysteresis window and saturation. Figure S2 exhibits the derivative of the I–V curves, dI/dV, shown in Fig. 2. The phase transitions occur at bias voltages where abrupt changes in dI/dV are observed.

To verify the proposed description of the switching mechanism, we analyzed the time-dependent heat dissipation in the device by solving the transient heat-diffusion equation. Calculations were performed for the specific layered structure of the experimentally tested devices, using the finite element method (COMSOL Multiphysics). The instantaneous Joule power generated in the channel is defined as $P(t) = V(t)I(t)$, where $V(t)$ is the applied potential, and $I(t)$ is the current in the 1T-TaS$_2$ channel.[57] The layered structure [see Fig. 1(d)] considered in the calculations includes the 0.5 mm-thick Si wafer, the SiO$_2$ gate dielectric, and the 1T-TaS$_2$ channel and metal electrodes. The through-plane thermal resistance of the Si/SiO$_2$ substrate includes three terms: $R_{th} = R_c + R_{SiO_2} + R_{Si}$, where R_c is the thermal contact resistance between the 1T-TaS$_2$ film and the SiO$_2$, and R_{SiO_2} and R_{Si} are the thermal resistances of the SiO$_2$ and Si layers, respectively. The thermal resistance of the SiO$_2$ layer is defined as $R_{SiO_2} = t_{SiO_2}/(k_{SiO_2} \times A)$, where t_{SiO_2} is the thickness (300 nm) of the SiO$_2$, k_{SiO_2} is its thermal conductivity, and A is the cross-sectional area of the channel. The interfacial contact resistance is $R_c = [G_{interface} \times A]^{-1}$ in which $G_{interface}$ is the interfacial thermal conductance and varies in a rather limited range for common 2D materials and substrates. For example, $G_{interface}$ for graphene, WTe$_2$, and MoS$_2$ with Si/SiO$_2$ substrates is 50, 33, and 15 MW/m^2 K, respectively.[65–68] Note that, for long current pulses, where the system is close to the steady-state condition, the average temperature rise in the device structure with SiO$_2$ layer rises to about $\Delta T \approx P \times R_{SiO_2}$, without even taking thermal contact resistance into account.[57] The temperature rise driven by the interfacial contact resistance can be as high as 100–200 K.[57,65,66]

Figures 3(a) and 3(b) present the results of simulations of the thermal profiles in a TaS$_2$ layer at the midpoint of 8 ns and 13 335 ns pulses, respectively. The dimensions of the channel are $W \times L \times t_f = 7\,\mu m \times 3\,\mu m \times 140$ nm, where W, L, and t_f are the width, length, and the thickness, respectively. The Joule heat generated by the pulse mostly diffuses through the underlaying SiO$_2$ layer owing to the substantial difference in the in-plane and through-plane thermal resistance. The in-plane thermal conductivity of 1T-TaS$_2$ is almost three folds higher than that of SiO$_2$.[69,70] However, owing to the small thickness of the 1T-TaS$_2$ channel, the total in-plane thermal resistance of the TaS$_2$ active layer, defined as $R_{th,in-plane} = L/(k_f \times t_f \times W)$, is approximately two orders of magnitude higher than the total through-plane thermal resistance, $R_{th,through}$, of the underlying SiO$_2$/Si layers. Consequently, almost all the generated heat is dissipated through the Si/SiO$_2$ layer as seen in Fig. 3. One can notice that the SiO$_2$ layer acts as an efficient thermal barrier owing to its small thermal conductivity and the thermal boundary resistance at the TaS$_2$–SiO$_2$ interface. While the heating is insufficient for 8-ns pulse duration [Fig. 3(a)] to drive the NC- to IC-CDW phase transition, by increasing the pulse duration to 13.3 μs the local temperature in the TaS$_2$ rises well above 350 K [Fig. 3(b)].
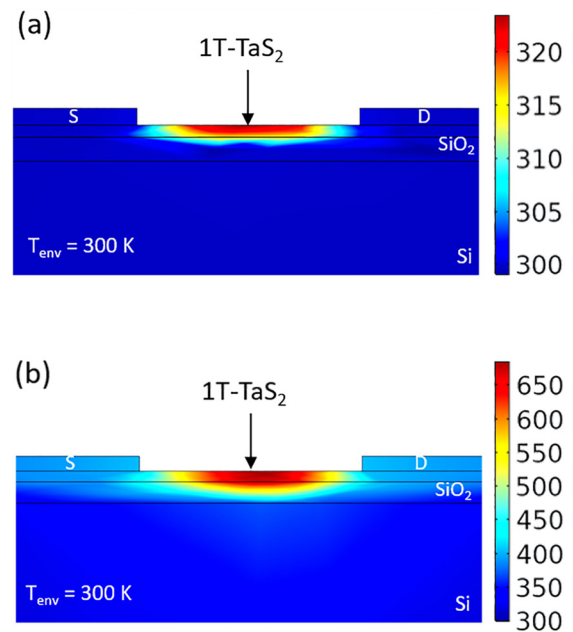

FIG. 3. Cross-sectional view of the simulated temperature distribution near the device channel, for applied current pulses of duration (a) 8 ns, and (b) 13 335 ns. In the case of the extremely short, 8-ns, pulses, the temperature of the film does not rise significantly above ambient, and remains below the NC- to IC-CDW phase transition temperature. For the much longer pulse, on the other hand, the temperature-rise is significant, exceeding this transition temperature.

To further support our interpretation of the experimental results, we have simulated the I–V curves of the device tested experimentally (see Fig. 4 and supplementary material Fig. S3). The pulse duration in these simulations was chosen to match the different values used in the experiments. The pulses were implemented in the model by applying them at various predefined ramp rates. The current at each time step was then calculated using the equations embedded in the COMSOL electromagnetic module. Additional simulation details are provided in the supplementary material. One can clearly see from Fig. 4 that the calculated trend for the evolution of the hysteresis is highly reminiscent of the experimentally measured one (see Fig. 2). This is due to the temperature rise in the 1T-TaS$_2$ which causes a drastic decrease in resistance [Fig. 1(a)] as a result of phase transition and, thus, an increase in the amount of current that passes through the channel.

For a quantitative comparison of the experimental and modeled trends, we define the width of the hysteresis ($V_{max} - V_{min}$) as the difference in the voltage values observed during the up and down ramps of the voltage at a constant current. This width is a meaningful parameter as it defines the operational range of voltages for CDW voltage-controlled oscillators and other types of switches. Measured and calculated values of this parameter, determined for a current of $I_{SD} = 8$ mA, are presented in Fig. 5. It is evident that both the experiment and simulations exhibit a peak at some particular value of the pulse duration, which should be defined by the interplay of the time constants for the generation and escape of heat. The absolute values of the measured and simulated hysteresis windows are different due to the fact that not all experimental factors, e.g., the heat dissipated to the
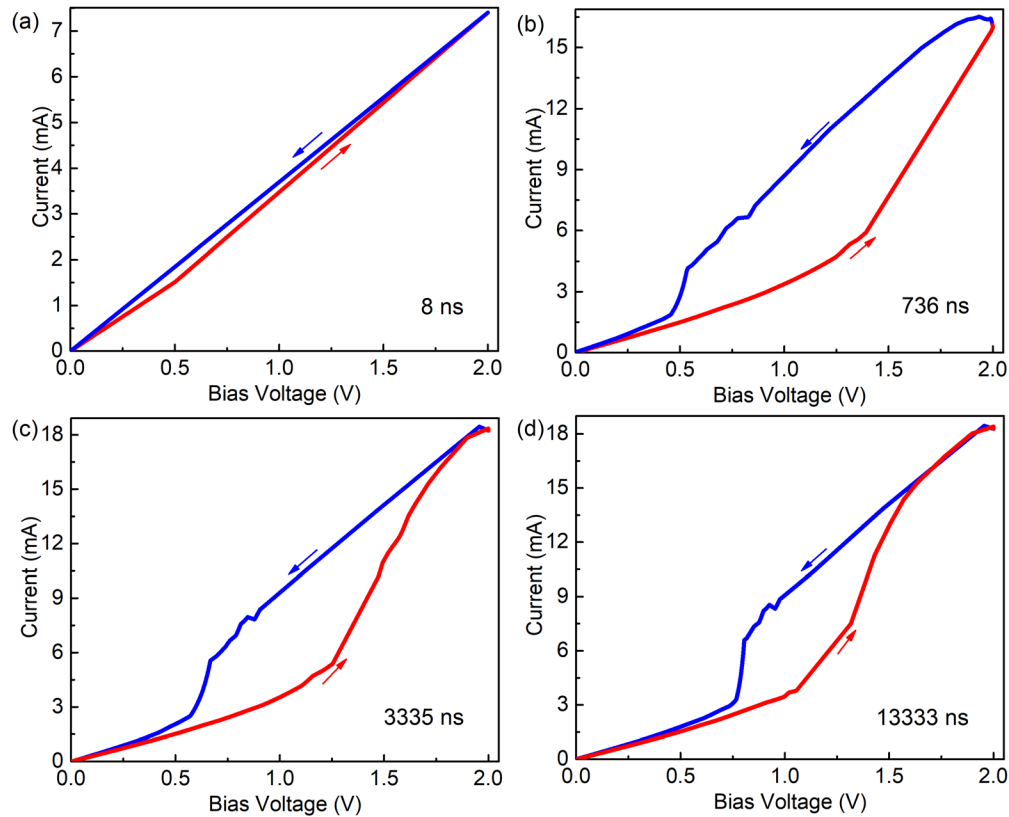
FIG. 4. Simulated pulsed-measurement results at pulse durations of (a) 8 ns, (b) 736 ns, (c) 3335 ns, and (d) 13 335 ns. The appearance, expansion and shrinkage of the hysteresis window follows the same trend as the experimental results. The ambient temperature is set at 300 K for these simulations.

environment, are accounted for in the simulation. The fine details of the position of the simulation data points, i.e., deviations from a smooth trend, are numerical due to the relatively coarse mesh used.

Our experimental results show that for the tested device the hysteresis window appears for a pulse duration of ∼200 ns. This corresponds to a CDW-device switching speed of ∼5 MHz. From the discussion above, it is clear that the speed can be increased if one optimizes the device structure and decreases its size to drive the desired phase transition by allowing heating to develop more rapidly. To demonstrate this point, in Fig. 6, we have used our experimentally validated physics-based model to simulate the I–V curves of a device with channel length, width, and thickness of 1 μm, 2 μm, and 10 nm, respectively. From this figure, one can see that the hysteresis appears at substantially shorter pulses than in Figs. 2 and 4. For a pulse duration of 20 ns, the calculated channel temperature reaches ∼360 K (see the supplementary material, Fig. S4), which is already above the NC to IC-CDW transition temperature. The hysteresis in fact begins to develop for pulses as short as ∼1 ns [see Fig. 6(d)], which corresponds to a CDW device speed of ∼1 GHz. The obtained data therefore suggest that CDW devices implemented with quasi-2D 1T-TaS$_2$ channels can operate at high frequency even if the NC-CDW to IC-CDW transition is thermally driven. We note that our study proves that this switching is achieved via thermal mechanism for the specific device design and characteristic thermal resistance of the structure. This does
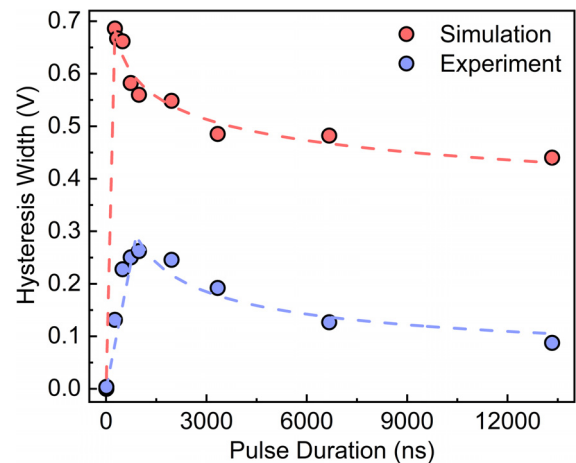

FIG. 5. Experimental and simulated hysteresis window width ($V_{cooling}$–$V_{heating}$) calculated at the constant current of 8 mA and as a function of pulse duration. The experimental and theoretical results both follow the same trend, exhibiting a peak at shorter pulse durations and approaching saturation at longer pulse times. The dash lines in the figure are guide for the eye.
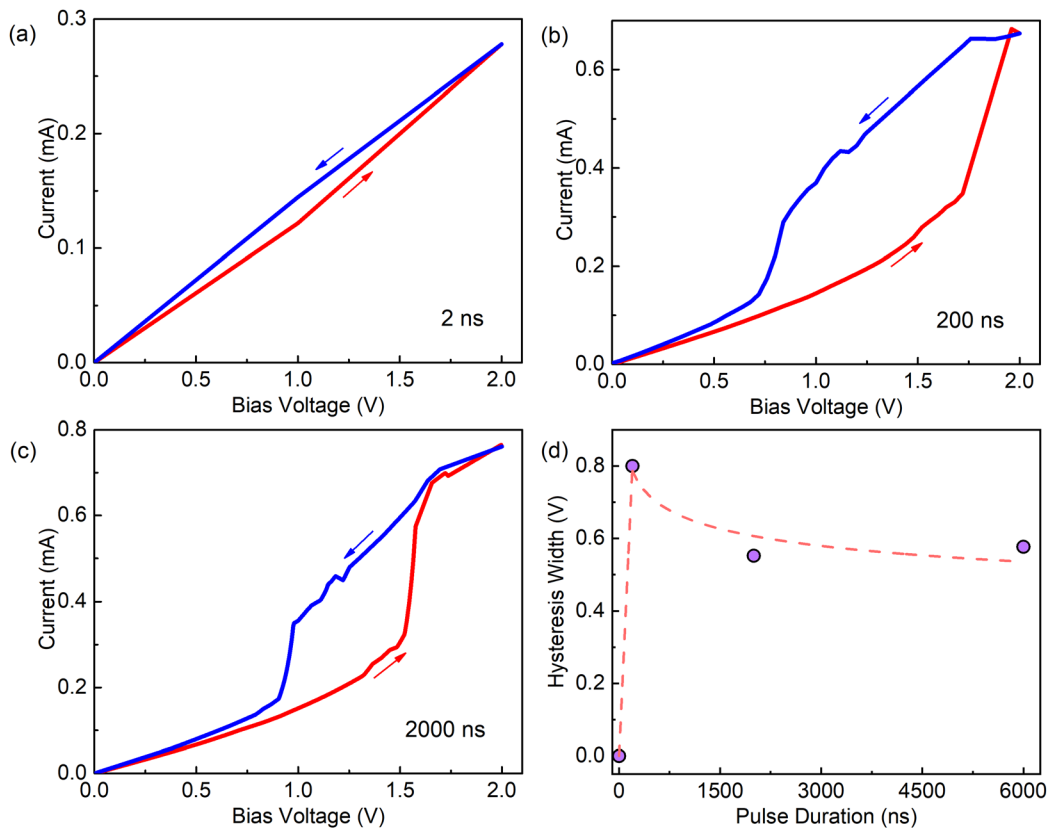
FIG. 6. Simulated pulsed measurement results for the projected device with smaller dimensions (the device length, width and thickness are 1 μm, 2 μm, and 10 nm respectively), at various pulse durations: (a) 2 ns, (b) 200 ns, and (c) 2000 ns. (d) Calculated hysteresis width for the same device as a function of pulse duration at constant current of 0.34 mA. The trend is similar to the previous experimental and simulation results. However, in this case, the hysteresis window can be observed even at smaller pulse durations. The hysteresis width has decreased compared to the larger devices. This confirms that, despite the dominant self-heating effect, careful tuning of the dimensions can lead to a device that can operate at GHz frequencies. The dash line in the figure is guide for the eye.

not preclude the possibility of purely electrically driven CDW transitions in other device designs and structures. If the pure-electric field regime is achieved, our estimates for the device operational speed should increase to even higher values.

In conclusion, we have reported on the room-temperature switching of 1T-TaS$_2$ thin-film CDW devices using nanosecond-duration electrical pulses. The switching action utilized the NC- to IC-CDW phase transition, which has a characteristic temperature of 350 K. The results of our rapid pulsed measurements, and numerical transient analysis of heat diffusion in the device structure, indicate the thermal nature of the switching in this type of CDW device. The modeling results suggest that a proper tuning of the device size and thermal resistance can allow these devices to operate at GHz frequencies even when the switching is thermally driven.

See the supplementary material for the details of device fabrication, finite element simulations, additional experimental and simulated current-voltage characteristics for different pulse durations, as well as differential current-voltage characteristics.

AUTHORS' CONTRIBUTIONS

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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